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AN INVESTIGATION OF THE USE OF

PARAMETRIC DIODES IN LIMITER CIRCUITS

A THESIS

Presented to

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by

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AN INVESTIGATION OF THE USE OF

PARAMETRIC DIODES IN LIMITER CIRCUITS

Approved:

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PREFACE

The general subject of this study, while rather broad in scope, has been restricted to one class of limiter circuits. While the analysis is not exhaustive, it is hoped that the information contained herein will be of value for outlining additional desirable areas of investigation and illustrating some limitations of the class of limiter circuits discussed.

Thanks are due Dr. W. B. Jones for his patience and advice, and to Dr. F. K. Hurd and Mr. W. B. Warren, Jr. for their helpful suggestions. I also wish to thank Mrs. R. A. Olson for her assistance in preparation of the manuscript, and all others who have contributed information and ideas.

The experimental portion of this investigation and part of the literature search was done in connection with Engineering Experiment Station project number E-231.

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SUMMARY

Many aspects of the use of voltage variable capacitance diodes as low noise circuit elements have been investigated since the advent of parametric amplification. However, there are still many areas of investigation which can contribute to the knowledge, and possibly to the usefulness of these devices. One such field of investigation is low level phase-distortionless "parametric" limiting. Limiting is said to occur when the output no longer increases with a further increase in input level.

There are basically two types of limiters which utilize parametric diodes. One uses a pump signal (local oscillator) in a conventional parametric amplifier circuit operated in a degenerate mode. The degenerate mode is said to exist when the circuit containing the parametric diode is pumped at twice its resonant frequency, or at the sum of the frequencies of the two tank circuits coupled by the parametric diode. The other type operates in a similar manner except that the signal supplies the power.

The latter type of limiter is considered in this investigation. Two circuits, one representing a shunt limiter and one representing a series limiter, are analyzed to determine the limiting characteristics and the effect of various parameters on these characteristics. The analysis shows that in the high-frequency region the input voltage required to achieve limiting is impractical to attain. Operation at frequencies of several kilomegacycles would be required before the

circuits could be operated at a practical input voltage level.

The shunt limiter and series limiter circuits were constructed to allow experimental validation of the results of the analysis. The experimental work was performed at 10 megacycles and at 30 megacycles. Although several different diodes were tried in the circuits and a wide range of bias values were used, as expected from the circuit analysis, limiting was not obtained.

Several additional circuits were experimentally investigated. Some of these circuits showed considerable promise as limiters.

The results of measurements of capacitance as a function of bias are presented. The experimental data are compared with the theoretical expression for capacitance as a function of voltage and an equation is derived which fits the experimental data. It is shown that in some cases the experimental data differ quite widely from the theoretical data. This effect is due to variation in the physical characteristics of the parametric diodes.

It is concluded that the series and shunt limiter circuits do not appear to be satisfactory for use in the high frequency range; however, other circuits showed considerable promise. The latter circuits warrant additional investigation.

CHAPTER I

INTRODUCTION

Increased interest in parametric devices has been evident in the past four years. These devices have been used for amplifiers, frequency control, multipliers, etc. However, there are still many areas of investigation in the parametric field which require additional work. Completion of the additional investigation will increase the knowledge concerning these devices, and possibly their usefulness. One such field of interest is limiting circuits which utilize semiconductor diodes having a voltage-variable capacitance characteristic. These diodes are called parametric diodes.

A parametric device can be defined as a device having a characteristic which varies with time in some manner. For such a definition it is useful and instructive to utilize differential equations. Consider a linear equation with variable coefficients in which the coefficients depend on the argument t, i.e., they are specific functions of time. In a physical sense, equations which have variable coefficients have parameters which vary with time in some respect. A system described by an equation of this type may be called a parametric system, and the action which takes place in them is called parametric. Parametric, then, denotes a system which has parameters that vary with time in some manner. The variation of capacitance in a parametric diode is usually assumed to be:

$$c(t) = C_o + Kv(t) \tag{1}$$

where $v(t)$ is a function of time, C_o is the static capacitance and K is a constant.

To fully understand limiting in a parametric device, it is necessary to understand the operating principles of a parametric amplifier. The parametric amplifier usually takes the form of either a modulator, a demodulator, or a negative resistance amplifier. This discussion will be restricted to the modulator or demodulator as defined by Manley and Rowe[1]. The amplification obtained in a parametric amplifier stage is a function of the pump frequency and the signal frequency and their amplitudes. It was deduced by Manley and Rowe[2] that the gain of a parametric amplifier is the ratio of the output to the input frequency, i.e.,

$$G_p = W_o/W_1 = f_o/f_i. \tag{2}$$

The deduction resulted from the consideration of the expressions for the interaction of two frequencies

$$\sum_{m=0}^{\infty} \sum_{n=-\infty}^{\infty} \frac{m\, W_{m,n}}{mf_1 + nf_o} = 0, \text{ and} \tag{3}$$

$$\sum_{m=-\infty}^{\infty} \sum_{n=0}^{\infty} \frac{n\, W_{m,n}}{mf_1 + nf_o} = 0\ . \tag{4}$$

These expressions are known as the Manley Rowe equations, where $W_{m,n}$ = average power flowing into the nonlinear capacitor at $f = \pm \left| mf_1 + nf_o \right|$. Also, + $W_{m,n}$ represents power into the system, - $W_{m,n}$ represents power out of the system, m and n represent integers (which may be positive or negative), f_1 represents the input frequency, and f_o represents the output frequency.

If we assume an input frequency of 100 megacycles and an output frequency of 2000 megacycles, we can obtain from Equation 2 that the theoretical gain is 2000/100, or a total theoretical gain of 20. The frequency may be determined from

$$f = \pm \left| mf_1 + nf_o \right| .$$

For example, if m = 1 and n = ± 1, the upper and lower sideband frequencies for the assumed input frequencies of 100 and 2000 megacycles are 2100 mcs and 1900 mcs, respectively. Using the assumed values for m, n, f_o, and f_1, Equation 3 can be written for the lower sideband as

$$\frac{- W_{1,-1}}{f_1 - f_o} ,$$

or Equation 4 may be written as

$$\frac{W_{1,-1}}{f_1 - f_o} .$$

If m = 2, then Equation 4 may be written as

$$\frac{2W_{2,1}}{2f_1 - f_o} .$$

Two important results of an analysis made by R.V.L. Hartley[3] in 1936, and which were considered in Manley & Rowe's derivation, are of importance in the consideration of limiting in circuits containing parametric diodes. These are:

(1) If a high and a low frequency source supply power to a reactance modulator unequally, the ratio of the two powers being greater than the ratio of the frequencies, then the higher frequency will supply most of the power and the low frequency source very little. Thus if it is assumed that the high frequency source is the pump and the low frequency source is the signal, it is seen that little power is required of the signal.

(2) The flow of power out of the modulator at the sum frequency is composed of power from both sources.

It may be said that a positive resistance is seen looking into both source circuits. However, the flow of power at the difference frequency introduces a positive resistance in the high frequency circuit and a negative resistance in the low frequency circuit.

The first result shows that it is possible to obtain a power gain with the high frequency oscillator supplying most of the power. The second result shows that it is possible, under certain conditions, to obtain instability or oscillation with only a local oscillator signal applied, and power extracted from all terminals. The extracted power may not be directly related to the pump (local oscillator frequency) but may be at any frequency determined by the tuning of the idler and signal circuits.

It is the second result which appears to be a useful tool in "limiting" applications. Assume a case in which the pump signal is the signal to be limited to a certain level. If the desired signal is extracted at the upper or sum frequency or at the signal frequency and the output at the lower or difference frequency (the frequency at which oscillation occurs) is dissipated, it becomes possible with suitable circuitry and proper biasing to limit the desired signal to a specific level. This is due to more power being extracted at the difference frequency after a critical level is reached than at the sum frequency. Adjustment of the bias should allow control of the level at which limiting occurs.

There are basically two types, or configurations, of limiter circuits which utilize parametric diodes. One type utilizes a pump signal (local oscillator) in a conventional parametric amplifier circuit operated in the degenerate mode. The degenerate mode exists when the circuit containing the parametric diode is pumped at twice its resonsnt frequency, or at the sum of the frequencies of two tank circuits coupled by the parametric diode. The other type uses only the signal to supply the power.

To explain the action of the first type of limiter, consider a parametric amplifier which can be considered either a modulator, a demodulator, or a mixer, with frequency translation taking place. Generally speaking, the flow of power at the difference frequency (lower sideband) introduces a positive resistance in the high frequency portion of the circuit and a negative resistance in the low frequency portion of the circuit. It is because of the latter effect that, under certain conditions, instability or oscillations occur and power may be extracted at the frequency of oscillation. The device will therefore act as a limiter after a certain level is reached since the additional power will be dissipated at the difference frequency. This type of limiter circuit has four frequencies involved, as shown in Figure 1, which are composed of the signal, pump, upper sideband and lower sideband.

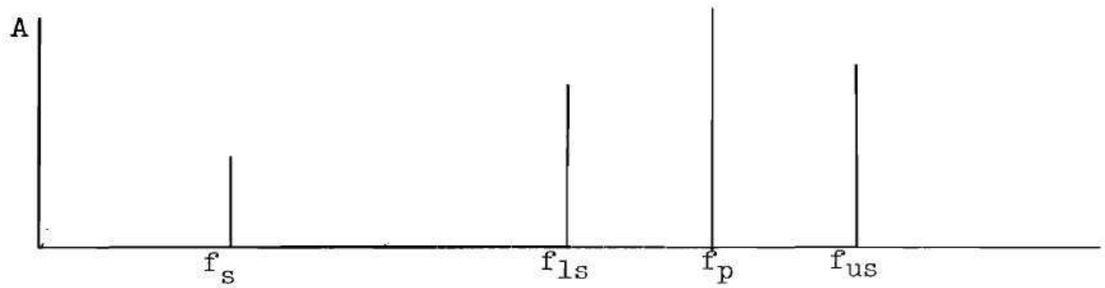


Figure 1. Frequency Composition of Limiters which Utilize Pump Signals.

Siegman[4] suggested that nearly ideal phase-distortionless limiting (above the threshold the output phase is constant) could be obtained by using the signal to be limited as the pump frequency in a parametric device, and by taking an output which is proportional to the response of the device to the signal. He stated the general principle as:

> The applied pump signal can be considered as a generalized force which, when applied to the parametric device, creates some sort of generalized motion. As the magnitude of the pumping force is increased, the corresponding motion is also increased, until it reaches that threshold value which is sufficient to set the parametric device into oscillation at some other and usually lower frequency or frequencies. The pumping motion then "sticks" at the threshold value, and further increases in pumping force, merely makes the device oscillate harder at other frequencies without increasing the amount of pump motion. If an output proportional to the pump motion is taken, the device will perform as an ideal limiter, limiting sharply at the threshold point.

Siegman gave an example of such limiting when using a ferrite parametric device, and he used a simple electromechanical model for analysis of the limiting characteristics. The resulting expressions show that above a certain threshold the motion of the capacitor is constant in both amplitude and phase, and the electrical oscillation amplitude is:

$$\bar{A}_1^{\,2} = 2K\,(F_m - 2\omega^2\,\bar{B}RK) \qquad (5)$$

where $\bar{A}_1$ is the oscillation amplitude, F_m is the mechanical driving force, $\bar{B}$ is the mechanical resistance or friction, R is the circuit resistance, K is a constant, and $2\ ^{2}\,\bar{B}RK$ is the threshold value of force necessary for electrical oscillations. He also states that all of the various forms of parametric amplifiers are potential limiters, but that further work will be necessary to see which is the most suitable. One serious limitation of his discussion is that the mass (inertia) of the capacitor plates is assumed negligible.

Olson, Wang and Wade[5] reported two parametric limiters of the first type using variable capacitance diodes which have been successfully tested for phase-distortionless limiting. One example, a device for limiting a 100 mc/sec signal, uses a 3300 mc/sec pump frequency. The 100 mc/sec signal is mixed with the 3300 mc/sec pump frequency in a variable capacitance diode to obtain upper and lower sidebands at 3400 mc/sec and 3200 mc/sec, respectively. The two sidebands are then mixed with the pump frequency to obtain an output at 100 mc/sec (the signal frequency). The output remained constant over an input range greater than 45 db. It was concluded from these results that some of the limiting in this particular device may be due to components in the system other than the parametric diode. Phase distortion in the system was difficult to measure; however, it was stated that little or no phase distortion was detected in the preliminary measurements.

The limiting characteristics of this device with respect to small-signal limiting are the best of any of these which have been found in the literature. However it has the disadvantage of requiring a pump signal at microwave frequencies, and an associated mixer.

Another parametric device described by Olson, Wang and Wade[6] is a simple S-band frequency converter with the limited signal obtained at the lower sideband frequency (2992 mc/sec). The input signal was at 2548 mc/sec, and the pump frequency at 5540 mc/sec. The authors conclude that limiting in this device is solely due to parametric action and the limiting in both devices exists in connection with a simple parametric frequency conversion. It was further concluded that the threshold curve exhibits the limiting characteristic; however, theoretical limiting is not as great as that observed experimentally. Equations derived as the result of an analysis of the equivalent circuit show that feedback between the pump and the input signal results in the output signal remaining constant although the available input power varies quite widely.

A plot of the output phase change as a function of the input level was said to be linear. A change of input level of one decibel caused an output phase change of approximately one degree.

Sutherland and Countiss[7] investigated an L-band limiter. In this limiter, three shorted coaxial transmission-line cavities are joined at a tee. A Microwave Assoicates MA460A VARACTOR was placed in shunt with all three cavities at their junction.

The dynamic limiting capabilities were determined using 1000mc/sec, 3-1/2 microsecond pseudo-Gaussian r-f pulses. The limiter was operated in the degenerate mode. (Both idlers were tuned to one-half the pump frequency.) The average input power was 280 mw and the peak input power was in excess of 15 watts. Provisions were made for biasing the parametric diode over the range ± 4 volts with suitable r-f bypassing.

Output power remained constant over a 30 db range of input power, and phase distortion over an input range of 16 db was found to be less than 2 degrees, which was the accuracy of the phase measurements.

It was concluded that the limiter operation is critically dependent on the tuning adjustment of all three cavities and also on bias adjustment. There was a broad combination of idler frequencies satisfying the relationship

$$f_3 + f_2 = f_p \tag{6}$$

such that limiting would occur. However, the best limiting action was found to occur when the limiter operated in the degenerate mode, where

$$f_3 = f_2 = f_p/2 \ . \tag{7}$$

The second type of limiter functions similarly to the first type except no local oscillator is used and the power is supplied by the signal only. In this limiter circuit the signal takes the place of the pump as shown in Figure 2.

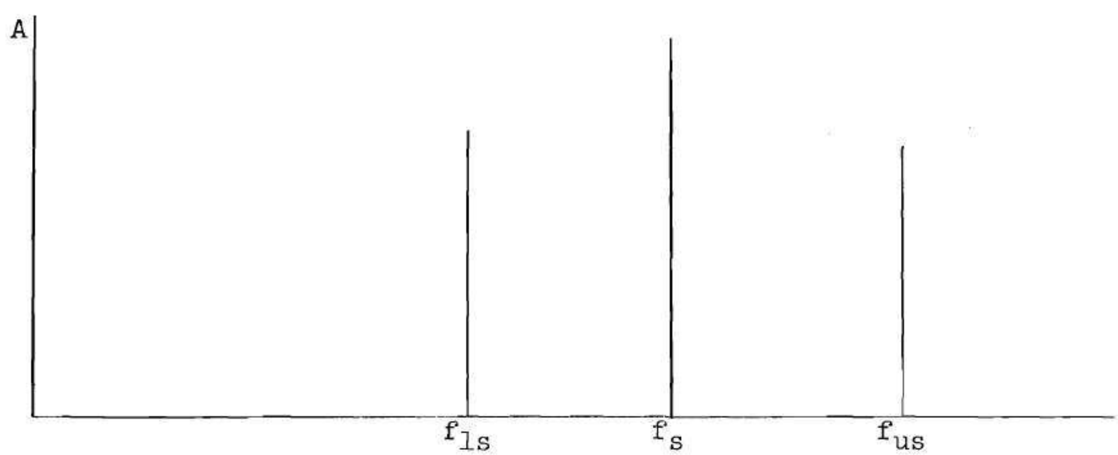


Figure 2. Frequency Composition of Limiters which Do Not Utilize Pump Signals.

It has been discovered that the most efficient limiter action occurs in the latter limiter when the undesired power is dissipated at the half frequency (where $f_{1s} = f_s/2$). Because of this effect the circuits in Figures 3 and 4 were selected for analysis and experimental determination of limiting characteristics.

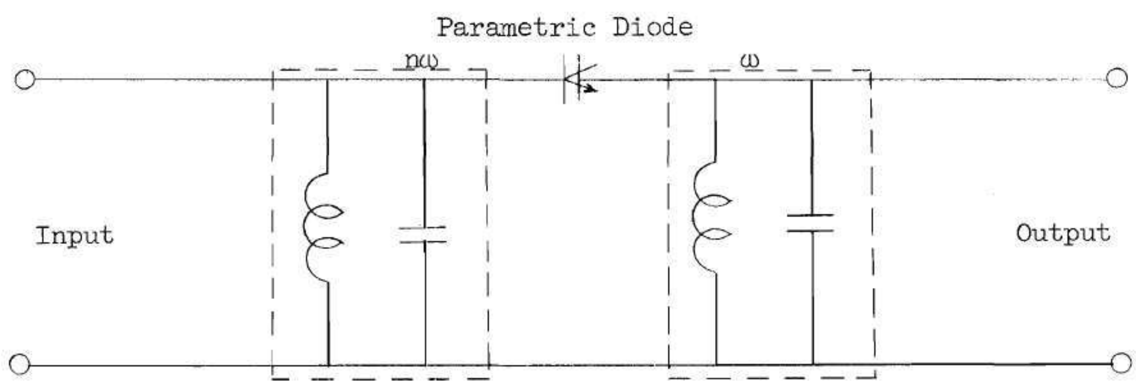


Figure 3. Series Limiter Circuit.

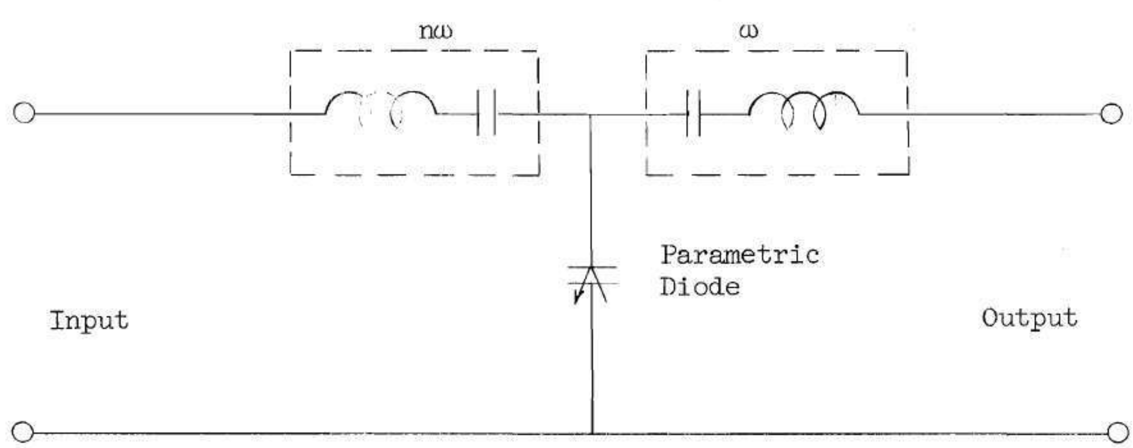


Figure 4. Shunt Limiter Circuit.

Louisell[8] explains the subharmonic oscillation which takes place with the following analogy:

> Consider a child on a swing. The child "pumps up" the swing amplitude by lowering his center of gravity on the downswing and raising it on the upswing. The "pumping frequency" is twice the swing resonant frequency, and energy is pumped into the swing amplitude. The raising and lowering of the center of gravity changes the effective length of the swing and is the time-varying circuit parameter that causes mixing between the two normal modes of the swing.
>
> The swing illustration is a degenerate case of two independent resonant circuits which are coupled by a time-varying parameter. If the pump is applied at a frequency equal to the sum of the frequencies of the two uncoupled circuits, the modes are coupled by the pump and energy is fed into both circuits.

It was the purpose of the investigation reported here to explore limiter circuits of the second type which utilize parametric diodes. The investigation has been restricted primarily to those circuits shown in Figures 3 and 4. These circuits have been analyzed and experimental data obtained. It has been determined that diode bias does not greatly affect the limiting action of the circuits which were investigated, but it does affect the point at which limiting occurs in some circuits and causes some variation in the limiting characteristic. Experimental techniques for evaluation of capacitance as a function of bias and limiting characteristics have been developed. These are discussed and illustrated in the following chapters.

CHAPTER II

PARAMETRIC DIODES

The parametric diode, so called because the capacitance can be made to vary as a function of time, is a semiconductor diode. Semiconductor diode theory, which has already been developed in great detail in a number of books and periodicals, explains the action which takes place. The capacitance variation in a semiconductor depends on the space charge in the transition region which ultimately depends on the flow of holes and electrons. The flow of holes and electrons depends on the voltage across the junction. Shockley[9,10] determined that the capacity for the neutral case ($K \ll 1$) is

$$C \cong \frac{\epsilon}{4\pi\ (4KL_0/10)} \tag{8}$$

where $K = L_0/2L_a$,

L_0 = the Debye length,

$L_a = n_i/a$,

n_i = electron density,

a = the constant gradient of the impurity density, and

ϵ = the dielectric constant.

Capacity for the space charge case ($K \gg 1$) is

$$C_{sc} = \frac{5\,\epsilon}{8\pi\ KL_0}\ . \tag{9}$$

It is further shown[11,12,13] that the transition region capacitance is:

$$C = \frac{\epsilon \underline{A}}{\left\{(12\epsilon/ae)[\Phi]\right\}^{\gamma} (1 - V/\Phi)^{\gamma}} = \frac{C_o}{(1 - V/\Phi)^{\gamma}} \qquad (10)$$

where C = the capacitance,

ϵ = the dielectric constant of the material,

γ = a constant determined by the junction characteristic,

V = the voltage across the junction,

$\underline{A}$ = the cross sectional area of the junction,

a = the constant gradient of the charge density,

Φ = the contact potential for the junction, and

e = the electronic charge.

For this derivation, the field at the boundaries of the space charge region was set equal to zero. However, it was shown by Uhlir[14] that consideration of the space charge field did not alter the form of the expression for graded junctions, but its consideration did indicate that the contact potential Φ has different values. The measured Φ was found to be consistently lower than the calculated Φ. In the case of indium antimonide junctions the discrepancy was found to be even larger. The value of the contact potential Φ has been found to be -1/2 volt for abrupt junctions, and -1/3 volt for graded junctions. Most of the parametric diodes available for use in this research are the abrupt junction type.

The capacitance of a parametric diode is relatively insensitive to temperature changes at the higher voltages; but due to variation of the contact potential it becomes increasingly sensitive to temperature as the voltage is reduced.

The capacitance ratio (ratio of the maximum to minimum capacitance) is limited by the breakdown (punch through) voltage, voltage sensitivity and the contact potential. The useful range is from a few tenths of volts in the forward direction, to the reverse voltage at which avalanche or punch through occurs. C(v) will be linear only to small signals. Large signals result in nonlinear effects which are useful in some applications, especially in limiting, harmonic and subharmonic generation.

Losses in parametric diodes are of critical interest in almost all applications. The major loss factor involved is the internal series resistance. This loss factor R_s and the capacitance are theoretically essentially frequency invariant up to several kmc; however, the losses do change with voltage across the junction. The inverse relationship

$$\frac{1}{2\pi f R_s C_s} \tag{11}$$

gives the figure of merit Q, where R_s is the series resistance, and C_s is the series capacitance. Experimental evidence indicates that the Q actually varies inversely with frequency up to several hundred megacycles and then remains relatively constant to several kmcs. Since the Q at lower frequencies, where measurements are usually made, depends on the frequency of measurement, it is not the best indication of parametric diode quality. A more general quality figure used is the "cutoff frequency."

$$f_c = \frac{1}{2\pi\ R_s C_s} \tag{12}$$

The cutoff frequency is the frequency at which Q would be unity on an extrapolated Q versus f plot. This is a more convenient specification because it does not depend on the measurement frequency.

The quality factor of the parametric diode is of importance in its application to limiters since it is shown that the threshold of oscillations depends to some extent on the losses involved.

Resonance Method of Measurement of Capacitance as a Function of Bias

There are a number of ways of measurement of the capacitance of a voltage variable diode as a function of bias; however, most conventional methods utilize an RX meter such as the Boonton 250A. Although the conventional methods were suitable for the measurement to be made in this investigation, a suitable RX meter was not available. It was therefore necessary to develop a method for rapid and accurate measurement of the desired characteristics utilizing available equipment.

A block diagram of the equipment arrangement is shown in Figure 5, and a schematic diagram of the test jig which contains the tuned circuit and bias bypass circuit is shown in Figure 6.

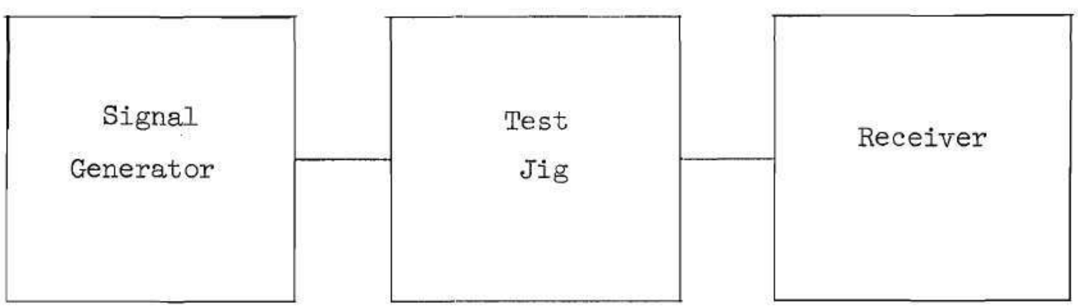


Figure 5. Equipment Arrangement for Measurement of Capacitance as a Function of Bias.

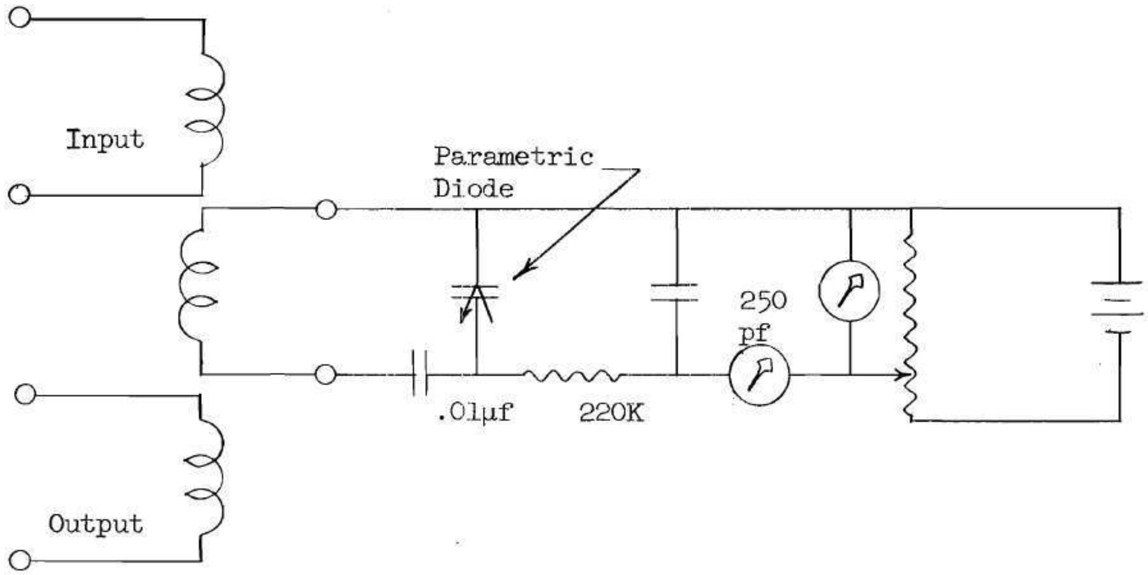


Figure 6. Schematic Diagram of a Test Jig for Measurement of Capacitance as a Function of Bias.

The signal generators used in these measurements are the Hewlett-Packard Models 606A, and 608A, and the receiver used is an Empire Devices Model NF-105 with the necessary tuning heads. However, any signal generator with the proper frequency range and a calibrated output and a receiver of the proper sensitivity and frequency range with an indicator and calibrated attenuator would be suitable.

The measurement of capacitance as a function of bias, using this method, is basically the measurement of the resonant frequency of a tuned circuit which has a known value of inductance. From the resonant frequency and known value of inductance, it is possible to calculate the capacitance quite accurately if the resonant frequency is low enough that stray capacitance does not have any appreciable effect.

Measurement Procedure.--The measurement procedure using the resonance method is given in the following steps.

1. With a known value of capacitance (silver mica) approximately equal to the nominal capacitance of the voltage variable capacitor, measure the resonant frequency of the test jig tuned circuit as specified in steps 2 and 3.

2. With a vacuum tube voltmeter connected to the test jig output, tune the signal generator to the estimated resonant frequency and adjust the signal generator output to obtain an indication on the voltmeter.

3. Adjust the signal generator tuning to obtain a maximum indication on the voltmeter, and with a frequency meter or the signal generator calibrating oscillator, accurately determine the signal generator frequency which gives the maximum indication.

4. From the known value of capacitance and the resonant frequency calculate the inductance (see Appendix A for an example).

5. Measure the 3 db bandwidth of the tuned circuit to allow determination of the circuit "Q" if desired.

6. Disconnect the voltmeter and connect the receiver.

7. Tune the signal generator to the nominal resonant frequency with the voltage variable capacitance in the circuit.

8. Adjust the receiver tuning to obtain a maximum indication on the output meter, and reduce the signal generator output until the indication is just above the receiver noise.

9. Adjust the variable capacitance diode bias to obtain a peak indication on the receiver output meter.

10. Measure accurately and record the signal generator frequency and the bias voltage.

11. Measure and record the 3 db bandwidth if desired with the bias voltage at the level recorded in step 10.

12. Adjust the signal generator frequency and repeat steps 8 through 11 at intervals sufficient to plot a smooth curve of capacitance versus bias. (See Appendix A for calculation of capacitance.)

RX Meter Method of Measurement of Capacitance as a Function of Bias

The RX meter method requires the use of an RX meter such as the Boonton 250A. It is necessary, regardless of which meter is used, that the measurement signal be less than 1% of the bias or 40 millivolts, whichever is greater. The Boonton 250A is well suited to this measurement since it has an adjustable signal voltage.

A test jig as shown in Figure 7 should be used with the RX meter for the following reasons: (1) the capacitance measurement range must be extended by suppressing the RX meter zero point; (2) the bias voltage must be isolated from the RX meter.

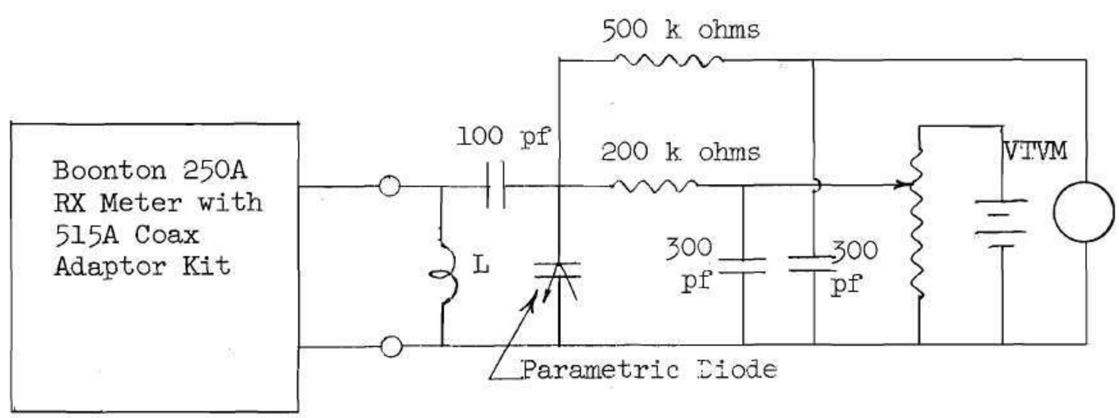


Figure 7. Test Jig for Use with the Boonton 250A RX Meter to Measure Capacitance at 50 Mc.

Suppression of the zero point is achieved with the one-half turn coil, L, (see Figure 7). The shape of the coil is adjusted in such a manner that the RX meter can be zeroed with the C_p dial at the -100 setting at 50 mc.

Voltage-variable capacitors may be tested at any dc bias voltage within their working voltage range; however, the 4 v value is accepted generally by the industry.

Direct readings in C_p and R_p are obtained with the RX meter. However, with the jig mounted on the RX meter terminals, correction and calibration charts have to be used to determine the series capacitance, C_s, and the figure of merit $\underline{Q}$, of the voltage-variable capacitor under test.

$$\underline{Q} = \frac{X_c}{R_s} = \frac{1}{\omega C_s R_s} \quad \text{or} \quad \underline{Q} = \frac{R_p}{X_c} = \omega C_p R_p \tag{13}$$

$$R_s = \frac{R_p}{1 + \omega^2 C_p{}^2 R_p{}^2} \cong \frac{1}{\omega^2 C_p{}^2 R_p} \tag{14}$$

$$C_s = \frac{1 + \omega^2 C_p{}^2 R_p{}^2}{\omega^2 C_p R_p{}^2} \cong C_p \tag{15}$$

From the above formulae it will be noted that $\underline{Q}$ can be calculated from either the series or parallel values, but as the RX meter gives the equivalent parallel values, we use these to determine $\underline{Q}$. The series resistance, R_s, may be subsequently determined from another chart.

The theory for the operation of the Boonton RX meter is discussed in the RX Meter Manual; therefore, it will not be considered here.

However, special properties of a non-linear impedance, such as a voltage-variable capacitor, when connected to the RX meter terminals should be reviewed.

In measuring a linear impedance, a wide range of signal voltages may be used. By looking at the capacitance versus bias voltage characteristics of a nonlinear capacitor it can be seen that a large signal voltage is undesirable because the changing impedance introduced by such a voltage swing gives a poor null indication and prevents accurate measurements. Averaging the high and low dial readings under such conditions does not give the true value. Therefore, it is desirable to use a small signal voltage. When using the test setup as recommended in these instructions, a signal voltage of approximately 40 mv is applied to the terminals of the voltage-variable capacitor under test.

<u>Preliminary Procedures</u>.--Mount the co-ax adapter kit to the RX meter as instructed in Appendix B of the meter manual and mount the test jig on the adapter so that the test jig terminals are at the right. Connect the bias supply and the VTVM. Set the C_p dial to "-100" and the R_p dial to "7K."

Set the oscillator range to 48 -110 mc and the oscillator frequency to 50 mc. Unbalance the bridge circuit by placing two fingers across the jig terminals, and adjust the detector tuning knob until a maximum deflection is obtained on the null indicator. Remove fingers and adjust the three zero balance controls until minimum deflection is obtained on the null indicator. (The preceding instructions are covered in the RX Meter Manual, and the manual should be referenced if one is not familiar with the meter.)

Measurement Procedure.--Connect the voltage-variable capacitor in the proper terminals on the jig (clip on or wire leads). Switch on the bias voltage supply and adjust to the correct bias value as monitored by the VTVM.

The C_p and R_p readings are obtained by first adjusting the C_p control to obtain an initial minimum, then adjusting the R_p and C_p controls alternately to obtain final balance. With the use of the charts, the C_p dial and the R_p dial readings are converted to the series capacitance and figure of merit.

Page 1 of the charts contained in the manual is used to obtain the C_s value from the C_p dial reading. Pages 2 and 3 give the actual parallel resistance, R_p, from the R_p dial reading. Page 4 gives the figure of merit, Q, from the computed C_s and R_p values. If the series resistance, R_s, is required, it can be obtained from page 5 using the computed C_s and Q values. Another method of stating the figure of merit of a voltage-variable capacitor is as the "cut-off frequency," f_c. This is the frequency at which Q would be unity on an extrapolated Q versus frequency plot. By using the Q value obtained from page 4 of the charts, f_c = Q x 50 mc. Sample calculation:

$$C_p \text{ dial reading} = -83.0$$

$$R_p \text{ dial reading} = 5.3 \text{ K.}$$

From page 1, C_s is found to be 23.0 pf. As this unit has wire leads, page 2 is used to find the actual R_p which is 17 K ohm. Q is 115, as determined on page 4. If R_s is required, page 5 gives the value of 1.2 ohm.

Experimental Results.--Measurements were made on five different diodes of the abrupt junction type using the resonance method. The results are given in Appendix B and Figure 8. In Figure 8 it is noted that the experimental values of capacitance as a function of bias differ appreciably from the theoretical values. However, an examination of other data in Appendix B indicates that for some parametric diodes the theoretical and experimental values are closely correlated. A curve fitted by a statistical method outlined in Appendix B is also plotted in Figure 8. It is seen that the curve thus derived, while showing good correlation at some points deviates quite widely at other points.

A correlation factor was applied to the theoretical expression for capacitance as a function of bias. The resulting equation was also plotted in Figure 8. It is seen that the points fall almost directly on the experimentally determined curve.

As discussed at the beginning of this chapter, the contact potential varies with each parametric diode. The variation is caused by differences in the diode junction. These differences are apparently due to the inability to control precisely each step of the manufacturing process. Since the corrected theoretical equation for capacitance as a function of bias is apparently a good representation of the capacitance, it is used in the limiter circuit analysis contained in Appendix C.

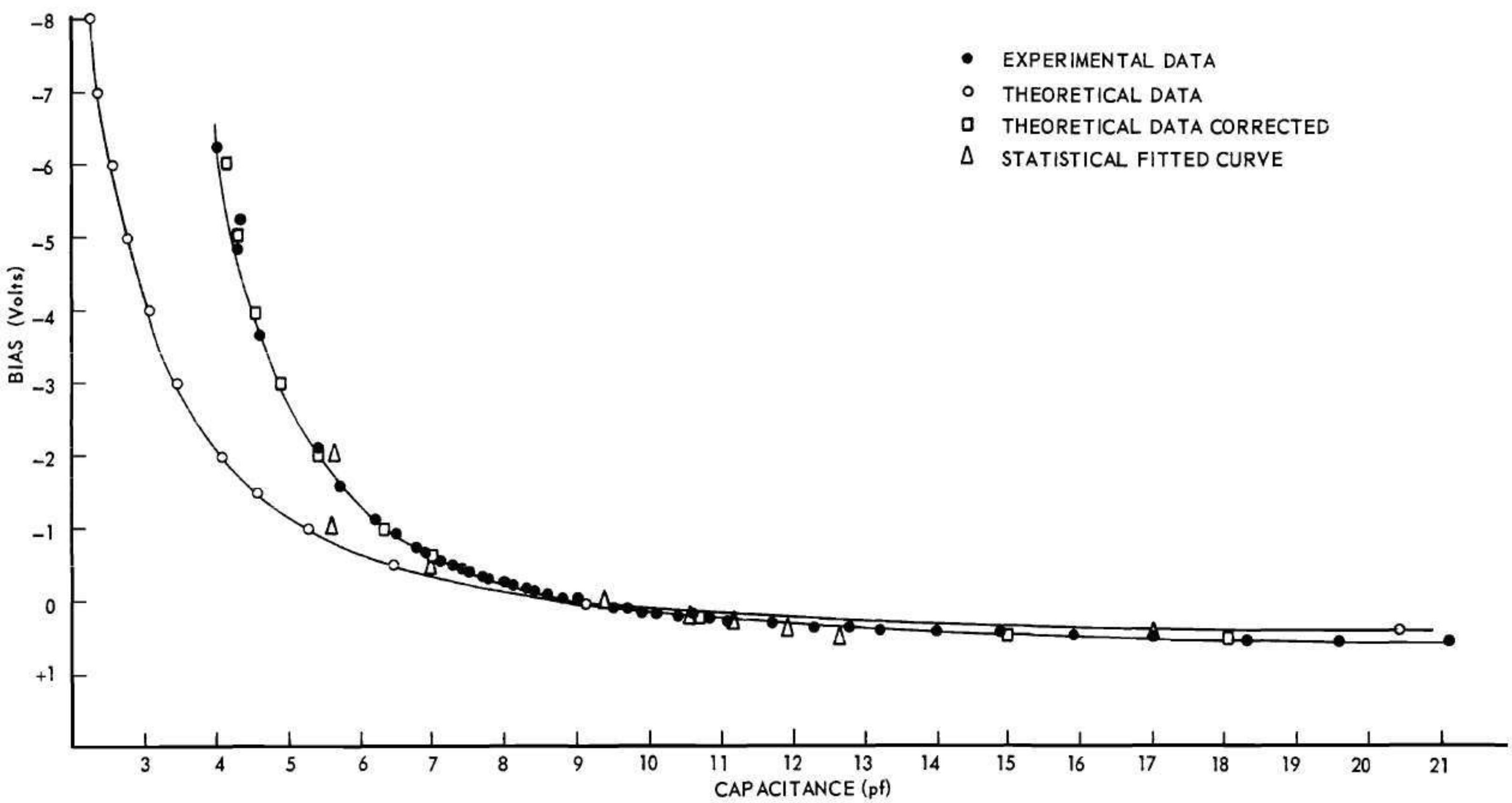


Figure 8. Capacitance as a Function of Bias for a PC-115-10 Parametric Diode.

CHAPTER III

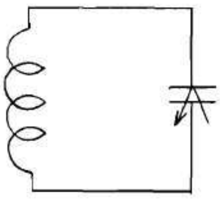
LIMITER CIRCUITS

Circuit Analysis

A number of different types of limiter circuits have been constructed which perform reasonably well at relatively high power levels in the microwave region as evidenced by the literature survey. However, much investigation remains to be done to determine optimum circuitry, type of nonlinear capacitor, bias level, etc., which are the most suitable for limiting applications. Little work has been done especially at low frequencies, and low power levels. However, since the quality factor changes inversely with frequency up to several hundred megacycles, it is expected that the limiting threshold would change with frequency.

The manner of operation of this type of circuit can be explained in the following way. A nonlinear circuit, i.e., a mixer, can cause mixing of two different modes of vibration (two frequencies); and an element, or parameter, which varies with time can also cause frequency mixing. In the mixing process energy supplied at one frequency can be converted to another. The coupling of modes by a time-varying circuit parameter is defined as parametric coupling.

The mechanism by which energy is coupled between modes by a time-varying parameter can be illustrated by the simple LC circuit of Figure 9. It is assumed for this example that the nonlinear capacitance is equivalent to a time varying capacitance given approximately by:



$$\omega = \frac{1}{LC_o}$$

Figure 9. Degenerate Parametric Oscillator.

$$C(t) = C_o + K \ \text{Cos}\ (\omega t + \theta)\ . \tag{16}$$

Assume that it is possible to mechanically change the capacitor plate separation at will. Since the capacitance depends on plate separation, i.e.,

$$C = \frac{\epsilon \underline{A}}{4\pi d} \tag{17}$$

where ϵ is a dielectric constant, $\underline{A}$ is the plate area, and d is the plate separation; the capacitor becomes a time varying parameter if the plate separation is caused to vary with time. Assume that the circuit is oscillating and the capacitor is fully charged. At the instant the capacitor becomes fully charged the plates are pulled apart. Since the plates are fully charged, work is required to separate them. The work increases the energy in the electric field between the plates, since the charge cannot change instantly. The instantaneous decrease in capacitance must then cause an increase in voltage ($V = Q/C$). After an elapsed time of one-fourth the resonant period, the capacitor has discharged and no energy will be required to restore the plates to the original separation. After another quarter period, if the plates are again pulled apart, more energy will be added to the circuit. It is then seen that if a signal at twice the tuned frequency of the circuit is applied, the oscillations at the resonant frequency, i.e., at one-half the pump frequency, can be made to grow. Theoretically the oscillations will grow without bound; however, circuit losses limit the amplitude.

There are several approaches which may be taken in the analysis of the circuits. The approach taken by Leeson[15,16] is to assume ideal filters; i.e., that series tuned filters will pass only those frequencies to which they are tuned and will reject all others, and that parallel tuned filters will reject frequencies to which they are tuned and pass all other frequencies.

Use of these assumptions and the assumption that the parametric diode operates in a purely capacitive mode results in a conversion efficiency for the equivalent circuit of Figure 3 given by[17]:

$$\frac{P_{n\omega}}{P_{\omega}} = \left(1 + \frac{G_a}{G_{in}}\right) \left(1 + \frac{G_b}{G_l}\right) . \qquad (18)$$

G_a is the equivalent output loss conductance due to the filter and parametric diode as seen from the load, G_b is the equivalent input loss conductance due to filter and parametric diode losses at the input frequency, and G_{in} is the input conductance.

The input conductance is given by:

$$\frac{\gamma\omega\, C_1 I_{in}}{G_l V_0} , \qquad (19)$$

where G_l is the total equivalent load conductance, γ is determined by the physical characteristics of the junction and lies in the range 0 to 1, C_1 is the capacitance at $V + \Phi = 1$ V_0 is the junction bias and I_{in} is the input current.

Since the input voltage,

$$E_{in} = \frac{I_{in}}{G_{in}} \quad , \tag{20}$$

which gives

$$E_{in} = \frac{I_{in}}{(\gamma\omega C_1 I_{in})/G_1 V_0} = \frac{G_1 V_0}{\gamma\omega C_1} \, , \tag{21}$$

the input voltage will remain constant and is independent of the input current. That is, the input voltage is limited to the value given by

$$G_1 V_0 / \gamma\omega C_1 \; . \tag{22}$$

The analysis also indicates that the efficiency and, therefore, the threshold of limiting for a given input and output conductance will be directly dependent on the loss conductance. Therefore, for high Q tuned circuits and parametric diodes, and low input and output conductance limiting at a low input voltage can be obtained. Theoretically, if the output conductance can be made small enough, limiting can be made to occur at an infinitesimally small voltage. However, this does not give the complete picture since loss terms are involved.

For the circuit of Figure 4, the dual of Figure 3, the current will be limited to:

$$I_{in} = \frac{4(\omega C_1)^2 \, R_1 V_0}{\gamma} \, , \tag{23}$$

where R_l is the lead resistance and the other parameters have the same meaning as in Equation 19.

The analysis of the limiter circuits which were selected for this study (contained in the Appendix) was made using assumptions similar to those of Leeson[18]. That is, it was assumed that the filters are ideal. It was also assumed that the input and output circuits are resonant at the desired frequency.

From the analysis (contained in Appendix C) thus made, using the stated assumptions and the experimental parametric diode characteristics, it was determined that the input voltage for the circuit in Figure 3 is given by:

$$E_{in} = \frac{[C' \ (1 - \gamma) + C_o{}'] \ G_1 V_o}{2\omega \ (C_o{}')^2 \ (1 - \gamma)^2} \ , \tag{24}$$

where C' and $C_o{}'$ are the experimentally determined values of capacitance, $\gamma = 1/2$, G_1 is the output conductance, and V_b is the bias voltage.

From the analysis it was also determined that the input current of the limiter circuit shown in Figure 4 is given by:

$$I_{in} = \frac{2V_o R_1 C_o{}' \quad [C' \ (1 - \gamma) + C_o{}']}{(1 - \gamma)^3} \ . \tag{25}$$

It will be noted that Equations 24 and 25 are very similar to those obtained by Leeson[19]. The difference may be attributed to the correction applied to the theoretical capacitance characteristic.

Equation 24 shows that if the circuit oscillates at the half frequency (ω), and a voltage exists at the half frequency, the input voltage will be limited to some value. The equation represents the value to which the voltage is limited. It also shows that the limit is directly proportional to the output conductance and bias voltage, and inversely proportional to the frequency and capacitance. Although, seemingly the bias may be varied over a wide range, in practice, the bias must be adjusted for the level at which best oscillations are obtained. That is, the bias must be adjusted to cause the circuit to oscillate.

If Equation 24 is evaluated for the PSI PC-115-10 parametric diode, it is found that the limit of the input voltage at 10 mcs is 1040 volts assuming that the output conductance is of the order of 10, the bias voltage is a few tenths of a volt, $\gamma = 1/2$, $C' = 2$ pf, and $C_o' = 7.1$ pf. For 100 mcs the limit would be 104 volts, and for 1000 mcs it would be 10.4 volts. Use of a larger capacitance, such as the Hughes HC 7005, or HC 7008 theoretically offers an improvement. The improvement is at a ratio approximately equal to the inverse square of the capacitance.

Measurement of Limiting.--The equation for use in measuring limiting characteristics is identical to that used in measurement of capacitance as a function of bias; however, in addition, a filter tuned to the limiter input frequency is used to isolate other frequencies from the input of the measuring devices. The equipment is arranged as shown in Figure 10.

Measurement Procedures.--

1. Connect the signal generator, limiter, filter and receiver as shown in Figure 9.

2. With the parametric diode unbiased (zero bias), and the input level at zero dbm, tune the receiver to obtain an indication at the

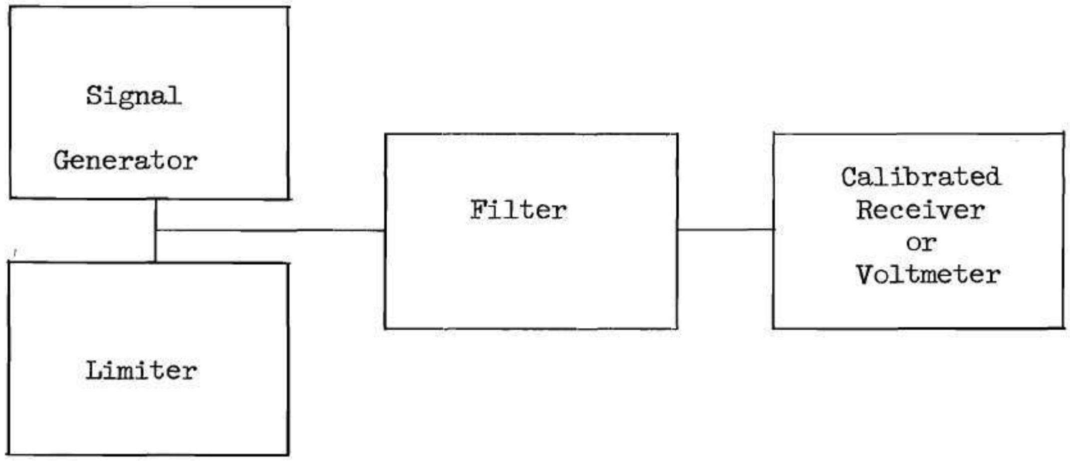


Figure 10. Equipment Arrangement for Measurement of Limiting.

input frequency.

3. Adjust the receiver attenuation to obtain an on-scale reading, and readjust the tuning to obtain a maximum indication.

4. Adjust the bias on either side of zero, and readjust the input level at which limiting occurs at the smallest input level.

5. Measure and record sufficient values of input and output to allow a smooth curve to be plotted. Record the bias level.

6. Select another bias value and repeat step 5.

Experimental Results for the Shunt and Series Limiters.-- The circuits of Figures 3 and 4 were constructed with low loss inductors and capacitors and arranged in a manner convenient for replacement of the parametric diode and determination of the limiting characteristics. An adjustable bias supply capable of supplying 45 volts dc was connected across the parametric diode to adjust the bias. The supply was radio-frequency isolated from the circuit to prevent interaction. Measurements were made at 10 megacycles and 30 megacycles input frequency. The bias was adjusted over a wide range in both cases, and the input voltage was adjusted for a maximum of three volts. As could have been predicted from the analysis results; it was not possible to obtain limiting in the circuits of Figures 3 or 4 even though the five diodes for which data are obtained in Appendix B and Figure 8 were tried in the circuits. Even if it were possible to obtain sufficient input voltage at the frequency of measurement, it would still not be practical to obtain limiting since the parametric diodes would not withstand the voltage.

Experimental Results for Other Circuits.--Since the series and shunt limiter circuits did not function as limiters in the high-frequency region, additional circuits were experimentally investigated. One such circuit was a variation of the circuit of Figure 3. The new arrangement is shown in Figure 11. With this arrangement excellent limiting characteristics were obtained, although a large amount of insertion loss was

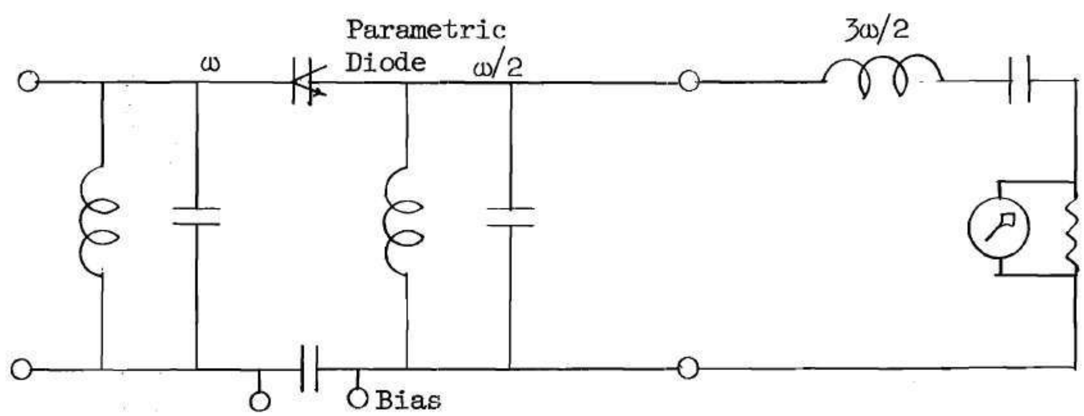


Figure 11. Degenerate Limiter.

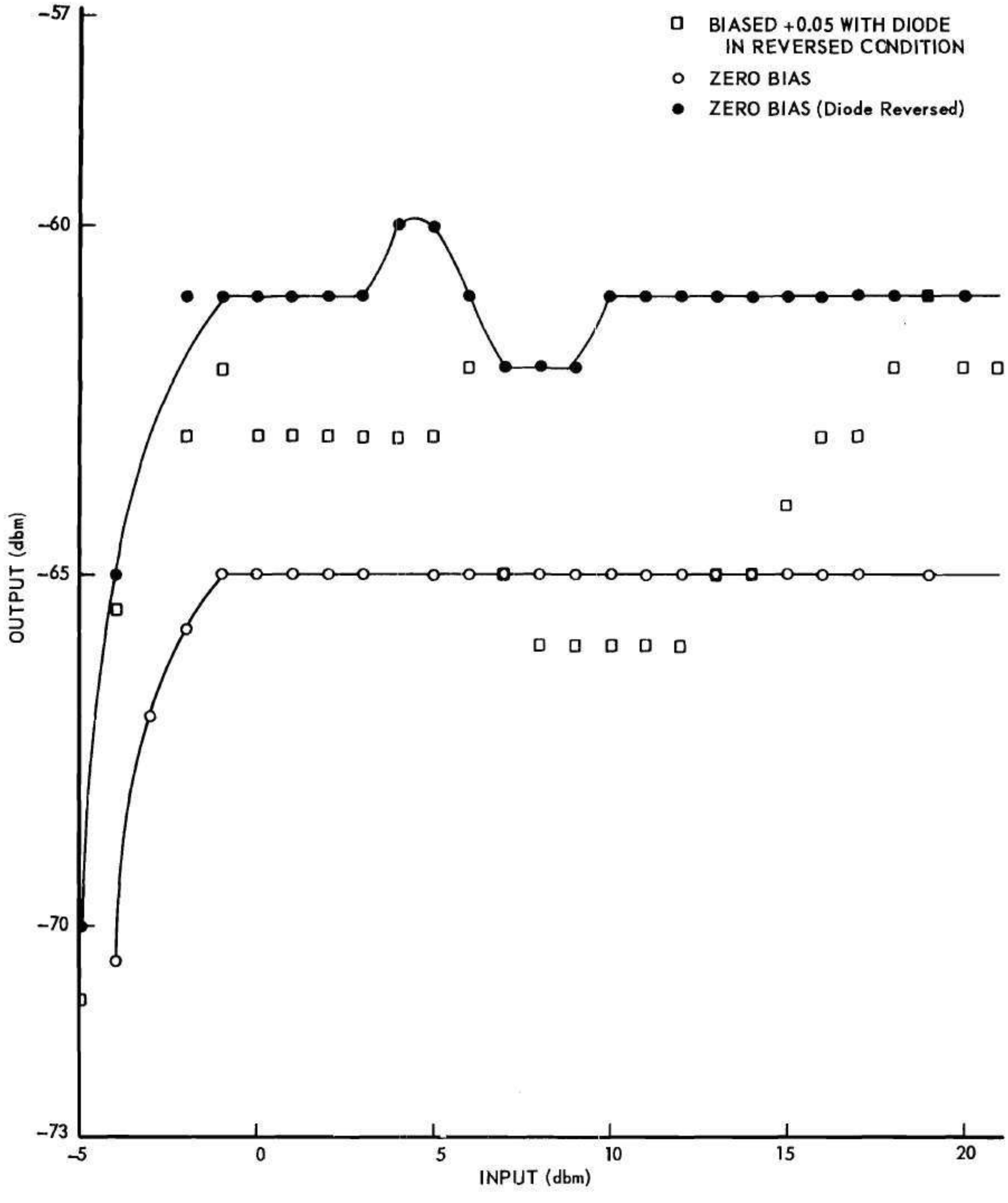


Figure 12. Output Characteristics of the Series Limiter Circuit Shown in Figure 11 with Output Taken at $3\omega/2$.

apparent. It is believed that this limiting resulted from two effects, (1) the oscillations produced a voltage at $\omega/2$, and also at 2ω, (2) the voltage at 2ω mixed in the nonlinear capacitor with $\omega/2$ to produce an output at $3\omega/2$, and (3) since the voltage at the lower sideband is inherently unstable the output at $3\omega/2$ was limited. The data obtained using the degenerate limiter is shown in Figure 12.

Another circuit, shown in Figure 13, was tried which showed much promise as a limiter in the high frequency range. When the input to the circuit of Figure 13 was at the frequency of the tuned circuit containing

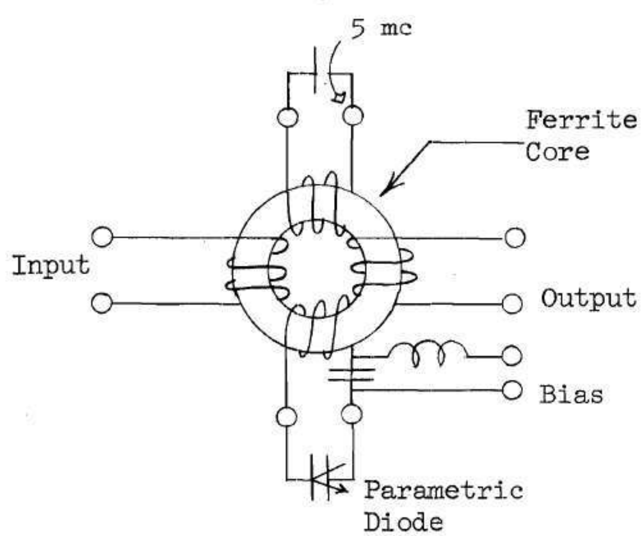


Figure 13. Experimental Limiter Circuit.

the parametric diode and the output was taken at twice the input frequency, limiting was initiated at approximately .05 volts. The bias was adjusted to cause the limiting to be initiated at the lowest possible level. For the particular circuit and diode the bias was -1.77 volts. If the output was taken at the input frequency, limiting occurred at an input voltage of .015 volts and a bias level of -0.03

volts. In both cases the circuit caused limiting over a range of input voltage of a maximum of 3 decibels.

The circuit was rebuilt to improve the wiring and the turns-ratio, and was readjusted. The output was then taken at twice the input frequency. It was observed that limiting began at an input voltage of less than 5 millivolts and with a bias level of -1.77 volts. The limiting was over a range of approximately 10 decibels.

Discussion of Experimental Results for the Series Limiter, Shunt Limiter, and Other Limiter Circuits.--The results of the analysis of the series and shunt limiter circuits, as evidenced by Equations 24 and 25, indicate that it is not possible to obtain limiting in the high frequency region; but limiting may be possible at frequencies of several kilomegacycles. As discussed in the experimental results, it was not possible to obtain limiting in the high frequency region. Due to equipment and facility limitations it was not possible to check the analysis results in the kilomegacycle region. It is possible, however, to conclude from the results that neither the series limiter or the shunt limiter are particularly adapted for use as a limiter in the high frequency region.

With the Pacific Semiconductors Incorporated parametric diode number PC-115-10 as the capacitive reactance portion of a tuned circuit, oscillations were obtained for an input of a few tenths of a volt. This indicates that it may be possible to obtain limiting if the diode is used as an active element of a tuned circuit and suitable filters are used.

The data shown in Figure 12 is interesting in that excellent limiting was obtained; however, the circuit would not be useful for some applications because no output would be obtained until the circuit begins to function at about -4 dbm input. Preamplification of the desired signal to insure that the circuit input is at an adequate level would solve the particular problem, but would limit the application of the circuit. For example, it could not be used at the input of a receiver to prevent distortion due to overloading because the preamplifier would be overloaded and the distortion would already exist prior to the limiter.

The circuit of Figure 13 showed promise as a limiter. It appears that by applying a signal at the resonant frequency of the circuit containing the nonlinear capacitor the circuit can be made to oscillate at a much lower input voltage. It was also apparent from the experimental measurements that frequencies were generated at one-half the input frequency and at twice the input frequency. However, it is not known whether the limiting is due entirely to the action of the parametric diode, or is a combination of effects due to the parametric diode and the ferrite core. At any rate the circuit exhibited the best limiting characteristics with respect to input level of any of those tried.

In the design and construction of the latter circuit it was observed that the external mutual coupling between circuits was critical, and shunt capacity affected the operation.

No attempt was made to measure the phase shift in any of the circuits, so it is not known at this time whether phase shift actually occurs or is significant.

CHAPTER IV

CONCLUSIONS AND RECOMMENDATIONS

As discussed in Chapter III, the series and the shunt limiter circuits examined do not appear to be suitable for use as limiters in the high frequency range. However, the circuit of Figure 11 shows promise as a limiter in this frequency range. It appears entirely possible to utilize a series of such circuits to obtain the desired limiting characteristic over a wide limiting range. It appears desirable to investigate the proposed series arrangement to determine if the desired limiting characteristics can be obtained by proper biasing.

Another approach, which shows a great deal of merit, is that of utilizing a pump signal to drive the parametric diode near the point of oscillation and to translate the input up in frequency. In theory at least the limiting should be made to occur at relatively low level.

Another field of investigation which deserves a great deal of effort is nonlinear circuit analysis. Although some effort has been devoted to this problem, and a large number of papers written on the subject, there are still many limitations which must be assumed to allow solution of the equations. Perhaps some new function must be defined and accepted to enable a more precise analysis. Until a more precise method of analysis is developed it does not appear necessary to obtain more exact equations for parametric diodes.

There are many aspects of the work and ideas presented here which could not be investigated because of equipment limitations and other considerations. Some of the questions arising are: What phase shift and distortion is experienced when limiting takes place? Is there an optimum frequency or frequencies for this type of limiter operation? How useful is this device when used as a conventional limiter?

These questions and the application of the parametric limiter to other uses are worthy of consideration. One application which has been suggested is the use of the limiter as an interference suppressor. In this application, a pump frequency, the amplitude of which is varied in proportion to the interfering signal, would be used. The varying amplitude would vary the level at which limiting would occur; thereby allowing the receiver to remain sensitive to the desired signal, but insensitive to the interfering signal.

APPENDIX A

CALCULATION OF CAPACITANCE

Calculation of Circuit Inductance.--The inductance of the tuned circuit which was used in the determination of diode capacitance as a function of bias may be calculated from the data obtained in the measurements outlined in the procedure of Chapter II. Figure 1A is a schematic diagram of the tuned circuit which was used in the experimental arrangement.

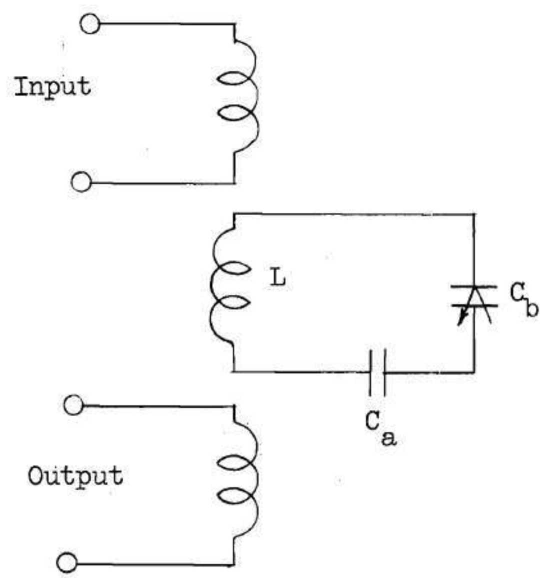


Figure 1A. Tuned Circuit for Capacitance Measurement.

To determine the value of L, C_b was replaced by a 20 pf silver mica capacitor, and the resonant frequency was found to be 26 mc/sec. The equation for the resonant frequency of a tuned circuit is:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad , \tag{1A}$$

and

$$C = \frac{C_a\ C_b}{C_a + C_b} \tag{2A}$$

therefore,

$$f = \frac{.159}{\sqrt{L\ \dfrac{C_a\ C_b}{C_a + C_b}}}$$

$$f^2 \left(L\ \frac{C_a C_b}{C_a + C_b} \right) = 0.253$$

$$L = \frac{.0253}{f^2} \left(\frac{1}{C_b} + \frac{1}{C_a} \right) \tag{3A}$$

Since $C_a \gg C_b$ (C_a = .05 mfd), an error of less than two percent will result if C_a is neglected since C_b is known to within one percent of its actual value. As in most measurements there is some observation error. Since the net effect of C_a is negligible when compared to other errors it will be neglected. The resulting equation is:

$$L = \frac{0.0253}{f^2 C_b} \tag{4A}$$

Substituting the values for f and C_b given previously

$$L = \frac{0.0253}{(26\text{x}10^6)^2 \text{ x } 20 \text{ x } 10^{-12}} = 1.87 \text{ microhenries.}$$

Calculation of Diode Capacitance.-- The diode capacitance may be calculated from the experimental data by use of Equation 4A; i.e.,

$$C_b = \frac{0.0253}{f^2 L} .$$

Since L is a constant and only f and C change

$$C_b = \frac{1.35 \times 10^{-4}}{f^2} . \qquad (5A)$$

Now if we assume that the resonant frequency with the parametric diode in the circuit is 10 mc, we obtain from Equation 5A

$$C_b = \frac{1.35 \times 10^{4}}{(10 \times 10^6)^2} = 135 \text{ pf}.$$

APPENDIX B

THE CAPACITANCE EQUATION AND EXPERIMENTAL VALUES OF CAPACITANCE AS A FUNCTION OF BIAS

Introduction.--The capacitance of a voltage variable capacitance diode varies essentially as $1/(V)^{1/2}$, where V is the voltage across the diode terminals. Diodes having a graded junction have a characteristic which differs from those having an abrupt junction. The expression for the capacitance of a graded junction is:

$$C(v) = \frac{C_o}{\sqrt[3]{1 - V/\phi}} \tag{1B}$$

but for an abrupt junction:

$$C(v) = \frac{C_o}{\sqrt{1 - V/\phi}} \tag{2B}$$

where V = dc bias voltage, C_o = capacitance at $V = 0$, and $\phi \approx 1/2$ volt.

Derivation of the Capacitance Equation.--What functional relationship, if any, exists between the junction capacitance and the bias across a parametric diode? One may use the theoretical relationship described in Equation 1B or 2B; however, it is apparent that the relationship cannot be predicted exactly in any particular case for a single diode, or for a large number of diodes because of the variation of contact potential, and other variations in the diode characteristics during the manufacturing process. One may consider an average relationship about which there is statistical fluctuation in particular cases, and then try to estimate this average relationship; or one may correct the theoretical expression by scrunity of the experimental data.

A common approach to this type of problem is to plot the data points on a graph, and then fit a smooth curve to the set of points. The resulting curve is an estimate of the underlying relationship. An estimate of the underlying relationship can be obtained by a statistical method using orthogonal polynomials as described in the Statistical Manual[21].

Example of Curve Fitting Method Using Statistics.--The results of measurement of the capacitance of a Pacific Semiconductor variable capacitance diode type PC-115-10 are shown in Table 1B. The results have been grouped into seventeen data points as shown in Table 2B to allow use of orthogonal polynomials found in Fisher's tables.[22] The values given in these tables are for polynomials evaluated at equal increments of one unit. Therefore, the experimental data must be adapted by changing the variable. For this case, let

$$X' = 3 - 10X.$$

The data points from the tables are shown in Table 2B for the first five polynomials. The ξ_is are shown in the table are orthogonal but not normalized. Therefore, the normalizing constants must be calculated before the $p_j(x)$ are obtained. These constants are given by

$$k_i^2 = \sum_{x=1}^{17} \Big(\xi_i(x) \Big)^2 \qquad (3B)$$

The results for this case are:

Table 1B. Experimental Values of Capacitance as a Function of Bias for a PC-115-10 Diode

Bias (V)	C (pf)
-6.25	4.00
-4.85	4.30
-3.70	4.60
-2.84	4.90
-2.14	5.30
-1.58	5.70
-1.40	5.90
-1.30	6.02
-1.20	6.12
-1.10	6.22
-1.00	6.35
-0.90	6.50
-0.80	6.65
-0.70	6.85
-0.60	7.10
-0.50	7.35
-0.40	7.70
-0.30	7.90
-0.20	8.35
-0.10	8.70
0.00	9.10
+0.02	9.30
+0.05	9.50
+0.10	9.80
+0.12	9.90
+0.14	10.10
+0.16	10.40
+0.18	10.60
+0.20	10.80
+0.23	11.10
+0.29	11.70
+0.33	12.40
+0.36	13.20
+0.38	14.00
+0.40	14.90
+0.48	15.90
+0.49	17.00
+0.52	18.30
+0.52	19.60
+0.54	21.20

Table 2B. Orthogonal Polynomials from Statistical Tables

x Bias(Volts)	x' Coded	y Cap.(pf)	$\xi_0(x)'$	$\xi_1(x)'$	$\xi_2(x)'$	$\xi_3(x)'$	$\xi_4(x)'$	$\xi_5(x)'$
+0.2	1	10.80	1	-8	+40	-28	+52	-104
+0.1	2	9.80	1	-7	+25	- 7	-13	+ 91
0.0	3	9.10	1	-6	+12	+ 7	-39	+104
-0.1	4	8.70	1	-5	+ 1	+15	-39	+ 39
-0.2	5	8.35	1	-4	- 8	+18	-24	- 36
-0.3	6	7.90	1	-3	-15	+17	- 3	- 83
-0.4	7	7.70	1	-2	-20	+13	+17	- 88
-0.5	8	7.35	1	-1	-23	+ 7	+31	- 55
-0.6	9	7.10	1	0	-24	0	+36	0
-0.7	10	6.85	1	1	-23	- 7	+31	+ 55
-0.8	11	6.65	1	2	-20	-13	+17	+ 88
-0.9	12	6.50	1	3	-15	-17	- 3	+ 83
-1.0	13	6.35	1	4	- 8	-18	-24	+ 36
-1.1	14	6.22	1	5	+ 1	-15	-39	- 39
-1.2	15	6.12	1	6	+12	- 7	-39	-104
-1.3	16	6.02	1	7	+25	+ 7	-13	- 91
-1.4	17	5.90	1	8	+40	+28	+52	+104

$k_0 = \sqrt{137}, \quad k_1 = \sqrt{408}, \quad k_2 = \sqrt{7,752}, \quad k_3 = \sqrt{3,876},$

$$k_4 = \sqrt{16,796}, \text{ and } k_5 = \sqrt{100,776}. \tag{4B}$$

The resulting normalized ploynomials are:

$$p_j(x) = \frac{\xi_j(X)}{k_i} \tag{5B}$$

$$p_0(x) = \frac{1}{\sqrt{137}}$$

$$p_1(x) = \frac{1}{\sqrt{408}} \quad (x - 9)$$

$$p_2(x) = \frac{1}{\sqrt{7,752}} \quad \left[(x - 9)^2 - \left(\frac{(17)^2 - 1}{12} \right) \right]$$

$$p_3(x) = \frac{1}{6\sqrt{3,876}} \left[(x - 9)^3 - (x - 9) \quad \frac{3(17)^2 - 7}{20} \right]$$

$$p_4(x) = \frac{1}{12\sqrt{2,002}} \quad \left[(x - 9)^4 - (x - 9)^2 \left\{ \frac{3(9)^2 - 13}{14} \right\} \right.$$

$$\left. + \frac{3(9^2 - 1)\ (9^2 - 9)}{560} \right] .$$

The best estimates of the $\hat{\alpha}_i$ are given by

$$\hat{\alpha}_i = 1/k_i \sum_{x=-4}^{4} y(x)\ \xi_i(x) \ .$$

The resulting $y(x)\xi_i(x)$ products are shown in Table 3B. The resulting $\hat{\alpha}_i^{\,2}$ are:

$$\hat{\alpha}_0^{\,2} = \frac{(127.41)^2}{17} = 954.9 \tag{6B}$$

$$\hat{\alpha}_1^{\,2} = \frac{(110.74)^2}{408} = 30.06$$

$$\hat{\alpha}_2^{\,2} = \frac{(143.36)^2}{7,752} = 2.651$$

$$\hat{\alpha}_3^{\,2} = \frac{(28.65)^2}{3,876} = 0.212$$

$$\hat{\alpha}_4^{\,2} = \frac{(31.03)^2}{16,796} = 0.057$$

$$\hat{\alpha}_5^{\,2} = \frac{(67.13)^2}{100,776} = 0.045.$$

These results may then be used to construct an analysis of variance (ANOVA) table such as that shown in Table 4B.

The F_i's resulting from the construction of such a table for this problem are:

$$F_0 = 86.92, \qquad F_1 = 78.11, \qquad F_2 = 6.97, \qquad F_3 = 0.56, \tag{7B}$$

$$F_4 = 0.17, \qquad \text{and} \qquad F_5 = 0.12.$$

The significant F level F^* is found to be 4.67 from Hald's tables[23]. Therefore, an examination of the computed list of F's show that only F_0, F_1, and F_2 are significant. The resulting equation for y is

$$\hat{y} = 10.977 - 0.603x + 0.0185x^2 \ . \tag{8B}$$

In terms of the original measured variables,

$$\hat{y} = f(x') = C(v) = 9.339 + 5.65v + 1.9v^2. \tag{9B}$$

<u>Correction of the Theoretical Equation</u>.--The theoretical equation may be corrected from experimental data by determination of the limit and a value C'. For this example the limit was found to be $\phi = 0.6$, and C' was found to be 2 pf. Where C' is the approximate difference in pf between the theoretical equation and the experimental data at a bias voltage of -10 volts. C_0' is then the difference between the experimental C_0 and the value of C'. The resulting equation is

Table 3B. The $y(x)\ \xi_i$ Products

x'	$y(x)$	$y(x)^2$	$y\xi_0'$	$y\xi_1'$	$y\xi_2'$	$y\xi_3'$	$y\xi_4'$	$y\xi_5'$
1	10.80	116.64	10.80	-86.40	432.00	-302.40	561.60	-1123.20
2	9.80	96.04	9.80	-68.60	245.00	- 68.60	-127.40	891.80
3	9.10	82.81	9.10	-54.60	109.20	63.70	-354.90	946.40
4	8.70	75.69	8.70	-43.50	8.70	130.50	-339.30	339.30
5	8.35	69.72	8.35	-33.40	- 66.80	150.30	-200.40	-300.60
6	7.90	62.41	7.90	-23.70	-118.50	134.30	- 23.70	-655.70
7	7.70	59.29	7.70	-15.40	-154.00	100.10	130.90	-677.60
8	7.35	54.02	7.35	- 7.35	-169.10	51.45	227.85	-404.30
9	7.10	50.41	7.10	0.00	-170.40	0.00	255.60	0.00
10	6.85	46.92	6.85	6.85	-157.60	- 47.95	212.35	376.75
11	6.65	44.22	6.65	13.30	-133.00	- 86.45	113.05	585.20
12	6.50	42.25	6.50	19.50	- 97.50	-110.50	- 19.50	539.50
13	6.35	40.32	6.35	25.40	- 50.80	-114.30	-152.40	228.60
14	6.22	38.69	6.22	31.10	6.22	- 93.30	-242.58	-242.58
15	6.12	37.45	6.12	36.72	73.44	- 42.84	-238.68	-636.48
16	6.02	36.24	6.02	42.14	150.50	42.14	- 78.26	-547.82
17	5.90	34.81	5.90	47.20	236.00	165.20	306.80	613.60
	$\Sigma y\xi_j^2$ ---	987.93	127.31	-110.74	143.36	-28.65	31.30	-67.13
		$C_i^2 = \sum_1^{17} \xi_j'^2$ --	17	408	7,752	3,876	16,796	100,776
			λ_j ---	1	1	1/6	1/12	1/20

$$C(v) = \frac{C' + C_o'}{\sqrt{1 - V/\Phi}} .$$

The data from the equation thus derived is plotted with the theoretical equation, the equation derived by statistical means and the experimental data in Figure 8, Chapter II. It is seen that the equation derived by the latter method fits the experimental data almost exactly.

Table 4B. Analysis of Variance Table (ANOVA)

Source (degree)	Degrees of Freedom	SS	MS	$F_{1,N-k-1}$
5	1	$\alpha_5{}^2$	$\alpha_5{}^2/1$	$\alpha_5{}^2/s^2$
4	1	$\alpha_4{}^2$	$\alpha_4{}^2/1$	$\alpha_4{}^2/s^2$
3	1	$\alpha_3{}^2$	$\alpha_3{}^2/1$	$\alpha_3{}^2/s^2$
2	1	$\alpha_2{}^2$	$\alpha_2{}^2/1$	$\alpha_2{}^2/s^2$
1	1	$\alpha_1{}^2$	$\alpha_1{}^2/1$	$\alpha_1{}^2/s^2$
constant	1	$\alpha_0{}^2$	$\alpha_0{}^2/1$	$\alpha_0{}^2/s^2$
error	13	S^2	$s^2=S^2/4$	
Total	17	Σy^2		

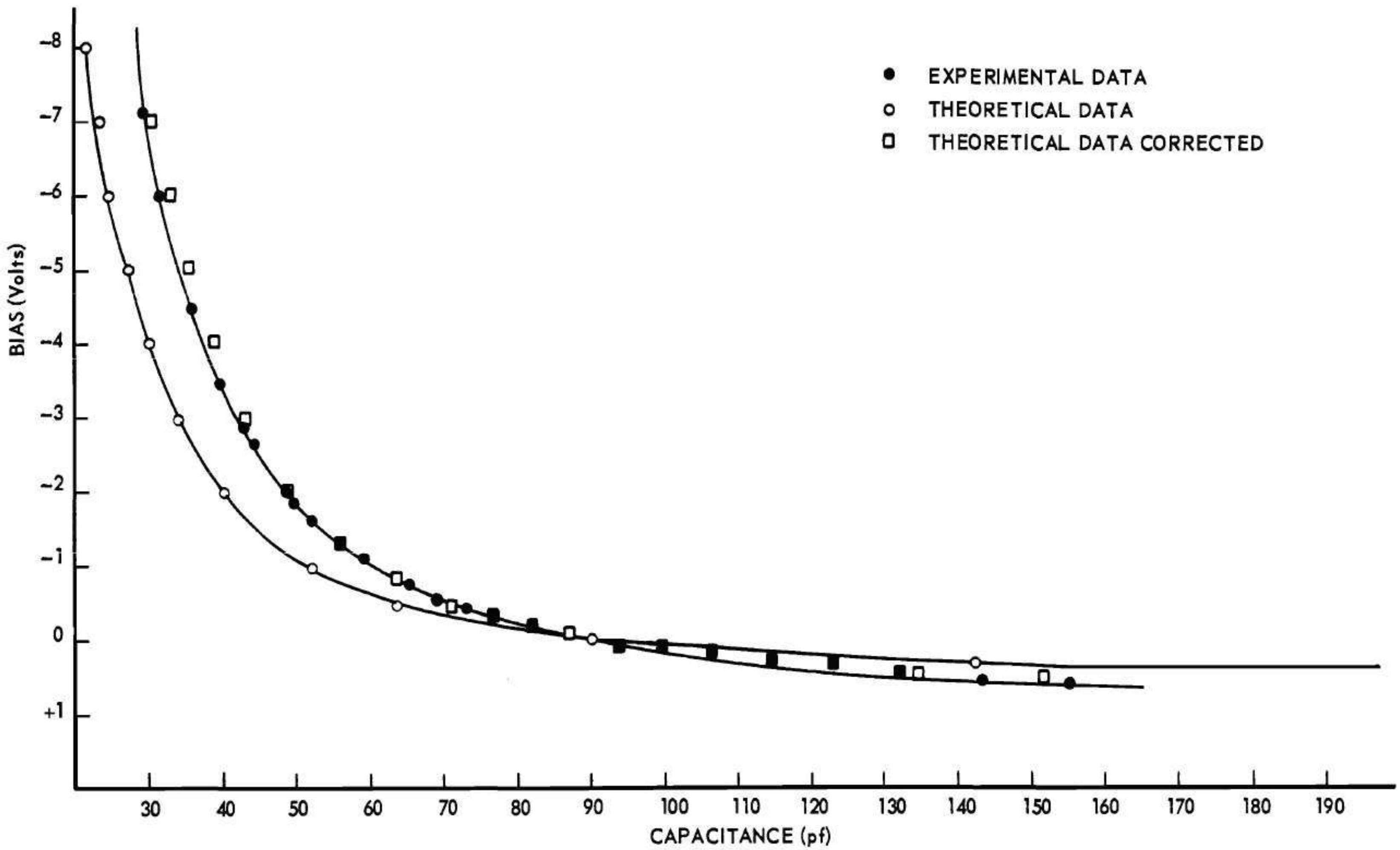


Figure 1B. Capacitance as a Function of Bias for a Hughes HC-7005 Parametric Diode.

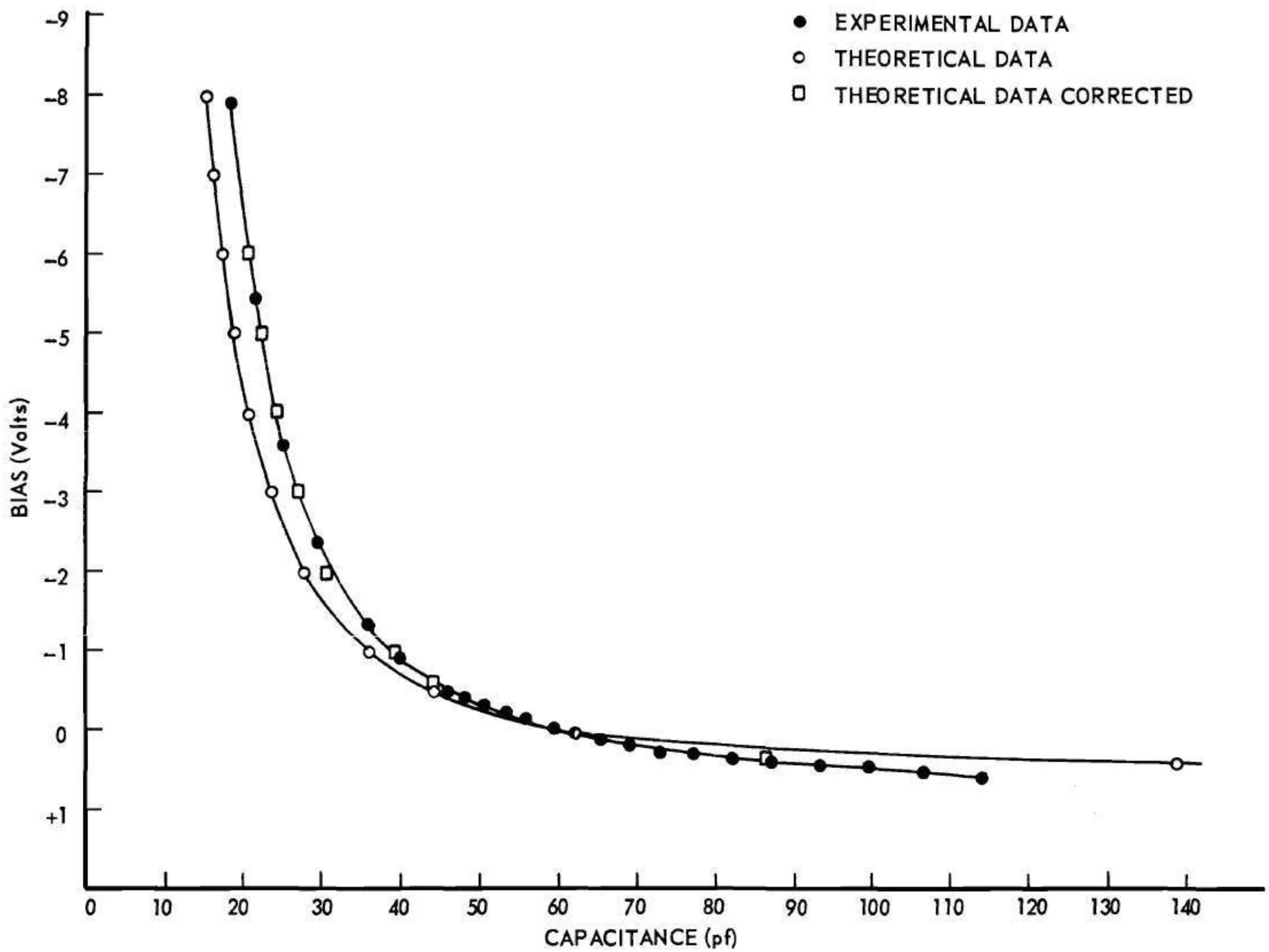


Figure 2B. Capacitance as a Function of Bias for a Hughes HC-7008 Parametric Diode.

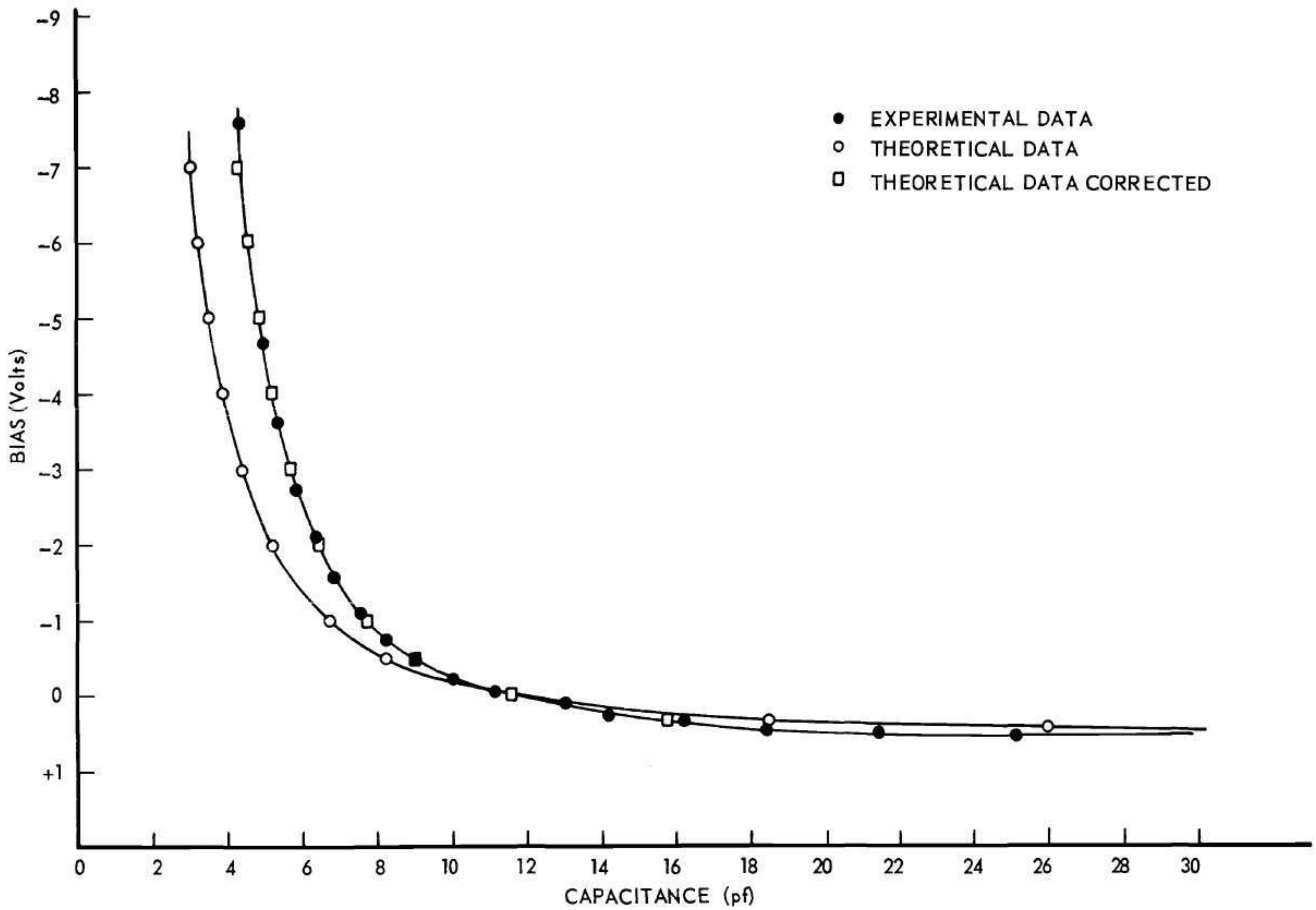


Figure 3B. Capacitance as a Function of Bias for a PSI VR-12 Parametric Diode.

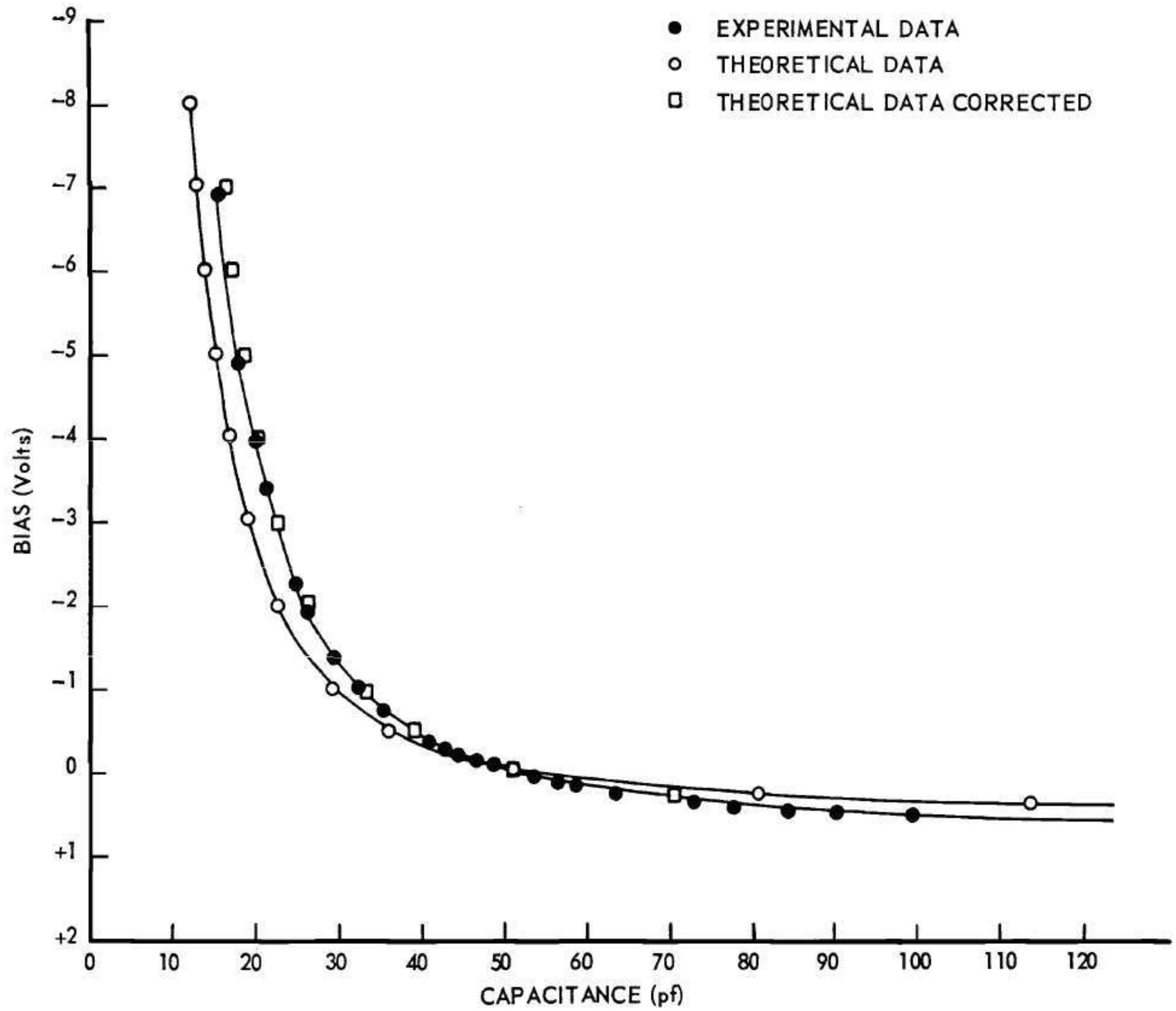


Figure 4B. Capacitance as a Function of Bias for a PSI PC-114-47 Parametric Diode.

APPENDIX C

ANALYSIS OF LIMITER CIRCUITS

Introduction.--The method used in the analysis of the limiter circuits is the same as that used by Leeson and Weinreb[24]. Initial assumptions are made that the following conditions are satisfied: 1) The nonlinear element and associated linear circuitry are lossless. 2) Power is dissipated in the load only at the desired harmonic or subharmonic frequency; and no power is dissipated in the source at any harmonic or subharmonic frequency. 3) The source is conjugate matched at its fundamental frequency. The first two conditions will be reconsidered later and corrections made to derived expressions.

Initially it will be shown how condition 3) can be met and after corrections are made it will be shown how limiting can occur in the circuits, and the expected limiting characteristics.

Analysis.--The first part of the analysis will be concerned with the series limiter circuit shown in Figure 1, and the second part with the shunt limiter circuit shown in Figure 3, Chapter III.

In the analysis it is assumed that the filters are ideal in that they are short circuits at all frequencies except the desired frequency in the case of Figure 1, or they are open circuits at all frequencies except the desired frequency in the case of Figure 2.

The Q-V relationship of the nonlinear element can be expressed in either of the following two functional forms:

$$Q = f(V) \tag{1C}$$

or

$$V = f(Q). \tag{2C}$$

The charge Q can be expressed as

$$Q = Q_o(1 + q) \tag{3C}$$

where Q_o is the quescent or dc operating point and q is the normalized variation of Q (the ac component). The total voltage can be represented by

$$V = V_o\ (1 + v) \tag{4C}$$

where V_o is the dc operating voltage, and v is the normalized variation in V (the ac component).

For the small signal case (1C) and (2C) can be expanded in a Taylor series around the dc (zero signal) operating point; resulting in

$$Q = f(V) = Q_o\ \ (1 + \alpha_1 v + \alpha_2 v^2 + \alpha_3 v^3 + \ldots) \tag{5C}$$

and

$$V = f(Q) = V_o\ (1 + \beta_1 q + \beta_2 q^2 + \beta_3 q^3 + \ldots) \tag{6C}$$

where the coefficients are evaluated by the following relations:

$$\alpha_k = \frac{V_o{}^k}{Q_o k!} \frac{d^k Q}{dV^k} \qquad \text{evaluated at } V = V_o \tag{7C}$$

and

$$\beta_k = \frac{Q_o{}^k}{V_o k!} \frac{d^k V}{dQ^k} \quad \text{evaluated at } Q = Q_o \ . \tag{8C}$$

If equations (3C) and(5C) are combined

$$Q = Q_o \ (1+q) = Q_o \ (1 + \alpha_1 v + \alpha_2 v^2 + \alpha_3 v^3 \ \ldots)$$

we obtain

$$q = \alpha_1 v + \alpha_2 v^2 + \alpha_3 v^3 \ \ldots = \sum_{k=1}^{\infty} \alpha_k v^k \ . \tag{9C}$$

If equations (4C) and (6C) are combined

$$V = v_o \ (1+v) = V_o \ (1 + \beta_1 q + \beta_2 q^2 + \beta_3 q^3 \ \ldots)$$

we obtain

$$v = \beta_1 q + \beta_2 q^2 + \beta_3 q^3 \ \ldots = \sum_{k=1}^{\infty} \beta_k q^k \ . \tag{10C}$$

Equations (9C) and (10C) are the general relations for the normalized ac variables, charge and voltage. These variables can be represented by their complex Fourier series:

$$q = \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} q_n t^{jn\omega t};$$

$$\frac{dq}{dt} = i = \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} i_n t^{jn\omega t} = \sum \ jn\omega q_n t^{jn\omega t};$$

$$v = \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} v_n \epsilon^{jn\omega t} \tag{11C}$$

where $n\omega$ is the driving radian frequency.

Since the currents and voltages are assumed to exist, they are real physical quantities; therefore, $v_{-n} = v_n^*$ and $q_{-n} = q_n^*$. If the variable v is put in the trignometric form

$$v = \sum_{n=1}^{\infty} |v_{trig}| \cos (n\omega t + \lambda),$$ (where λ is the phase relationship)

it follows that

$$|v_{trig}| = |v_n| + |v_{-n}| = 2 |v_n| .$$

The quadratic and cubic terms for v^k appearing in equation (9C) in the form of Fourier Series are:

$$v^2 = \sum_{n=-\infty}^{\infty} (v^2)_n \epsilon^{jn\omega t},$$

where $(v^2)_n$ can be written as

$$(v^2)_n = \sum_{\substack{j, \ell = -\infty \\ j+ \quad = n}}^{\infty} v_j v_\ell$$

and

$$v^3 = \sum_{n=-\infty}^{\infty} (v^3)_n \epsilon^{jn\omega t},$$

where $(v^3)_n$ can be written as

$$(v^3)_n = \sum_{\substack{j,\ell,m=-\infty \\ j+\ell+m=n}}^{\infty} v_j v_\ell v_m . \tag{12C}$$

It will be noted that all possible permutations have to be considered to calculate any one of the Fourier coefficients. $(v^k)_n$ is the sum of all combinations of products of k voltages whose indices add up to n.

To simplify further analysis we will assume that only the fundamental and subharmonic voltages are present, and therefore, all voltages except $v_{\pm 1}$ and $v_{\pm n}$ are zero. This will allow calculation of $(v^k)_n$ in terms of $v_{\pm 1}$ and $v_{\pm n}$ only; with the introduction of the load constraint, $i_n = jn\omega q_n = -v_n y_n$, (where y_n is the normalized load admittance at the subharmonic frequency). q_1 and q_n can then be calculated in terms of v_1.

Solving for q_n in the form of equation (12C), we obtain

$$q_n = \alpha_1 v_n + \alpha_2 \sum_{\substack{j+\ell=n \\ |j|,\,|\ell|=1 \text{ or } n}} v_j v_\ell + \alpha_3 \sum_{\substack{j+\ell+m=n \\ |j|,\,|\ell|,\,|m|=1 \text{ or } n}} v_j v_\ell v_m + \ldots \tag{13C}$$

If we consider each of the terms in (13C) we see that the expression must produce factors of the form

$$v_n(v_1 v_{-1}),\ v_n(v_n v_{-n}),\ v_n(v_n v_{-1}{}^n),\ v_n(v_{-n} v_1{}^n)$$

or

$$v_1{}^n(v_1 v_{-1}),\ v_1{}^n(v_n v_{-n}),\ v_1{}^n(v_n v_{-1}{}^n),\ v_1{}^n(v_{-n} v_1{}^n)$$

so that the summation of the product indices will equal n. Furthermore, all additional terms must produce products of the same form to satisfy the equality. Therefore, we can represent the complete series by terms of the following two types:

$$1)\quad v_n \left\{ (v_1 v_{-1})^a \, (v_n v_{-n})^b \, (v_n v_{-1}{}^n)^c \, (v_{-n} v_1{}^n)^d \right\}$$

where a,b,c,d are zero or a positive integer. The total number of terms k can be obtained by summing all of the products. For the first factor there will be 2a terms since there are two voltages raised to the a-th power, for the second factor there will be 2b terms, the third (n+1)c terms, and the fourth (n+1)d terms.

Therefore,

$$2a + 2b + (n+1)c + (n+1)d = K.$$

If $k < n + 2$ both c and d must equal zero.

$$2)\quad v_1{}^n \left\{ (v_1 v_{-1})^a \, (v_n v_{-n})^b \, (v_n v_{-1}{}^n)^c \, (v_{-n} v_1{}^n)^d \right\}$$

and by the same reasoning as above,

$$2a + 2b + (n+1)c + (n+1)d + n = K$$

Where n results from the fact that if a,b,c,d are zero there will be n terms remaining due to $v_1{}^n$. If $K < 2n + 1$ again c and d must be zero.

By the assumptions made previously that v_1, V_o, and Q_o are positive real, and $v_{-1} = v^*$, $v_{-n} = v^*$, the quantities $(v_1 v_{-1})$, $(v_n v_{-n})$ and α_k are positive real. If $K < n + 2$ then all coefficients of v_n must be positive real since the coefficients will contain only factors involving $(v_1 v_{-1})$ and $(v_n v_{-n})$. Likewise, if $K < 2n + 1$, $v_1{}^n$ will have only positive real coefficients.

As a result we can write (13C) in terms of the two voltages v_n and $v_1{}^n$ in the form:

$$q_n = A\ v_n + B\ v_1^{\ n} \qquad (14C)a$$

where terms for $k > n + 2$, and $k > 2n + 1$ are neglected which leaves only positive real quantities.

The current ($i_n = jn\omega q_n$) due to the first term of (14C) is in quadrature with v_n. This means that there is no contribution to exchange of power by the first term, but it represents reactive power only. The second term, however, represents an independent current source since it is in terms of the input voltage.

Under the assumptions of small signal analysis we can limit the first and n-th frequency components of (9C) and (10C) to a small number of terms and complete the analysis.

<u>Analysis of the Series Limiter Circuit</u>.-- The solution leading to the circuit equation for the series limiter circuit involves the solution for the various charges (equation 9C) in terms of the driving voltage.

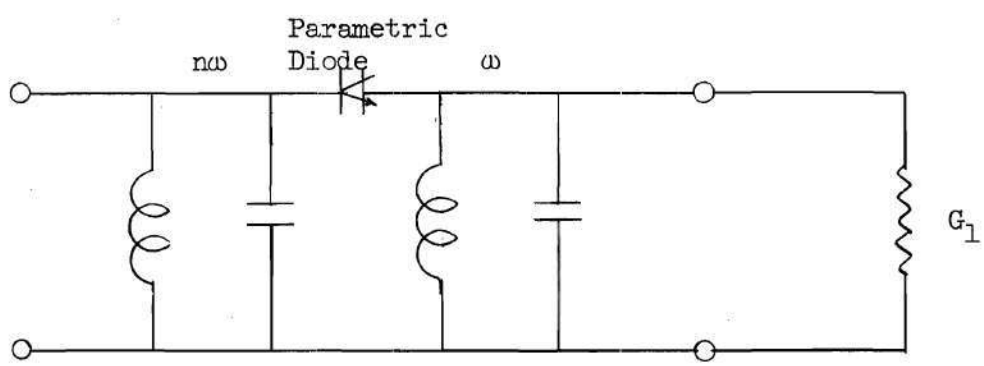


Figure 1C. Series Limiter Circuit.

Since we have concluded that we need only consider the first and n-th terms of Fourier Series for the charge, it reduces to

$$q = \alpha_1 v + \alpha_n v^n \ . \tag{14C)b}$$

Now v_n can be replaced by its complex Fourier Series represented by (12C). This gives

$$q_1 = \alpha_1 v + \alpha_n (v^n)_1 \tag{15C}$$

and

$$q_n = \alpha_1 v_n + \alpha_n (v_1^n)_n \tag{16C}$$

where (15C) is the first term of the series and (16C) is the n-th term.

If we separate (15C) and (16C) into real and imaginary components by making small signal approximations and allowing $v_1 = v_{-1}$, and specifying v_1 to be real; we obtain

$$q_{1_r} = \alpha_1 v_1 \tag{17C}$$

$$q_{1_i} = n\alpha_n {v_1}^{n-1} v_{n_i} \tag{18C}$$

$$q_{n_r} = \alpha_1 v_{n_r} + \alpha_n {v_1}^n \tag{19C}$$

$$q_{n_i} = \alpha_1 v_{n_i} \tag{20C}$$

where the subscripts r and i refer to real and imaginary.

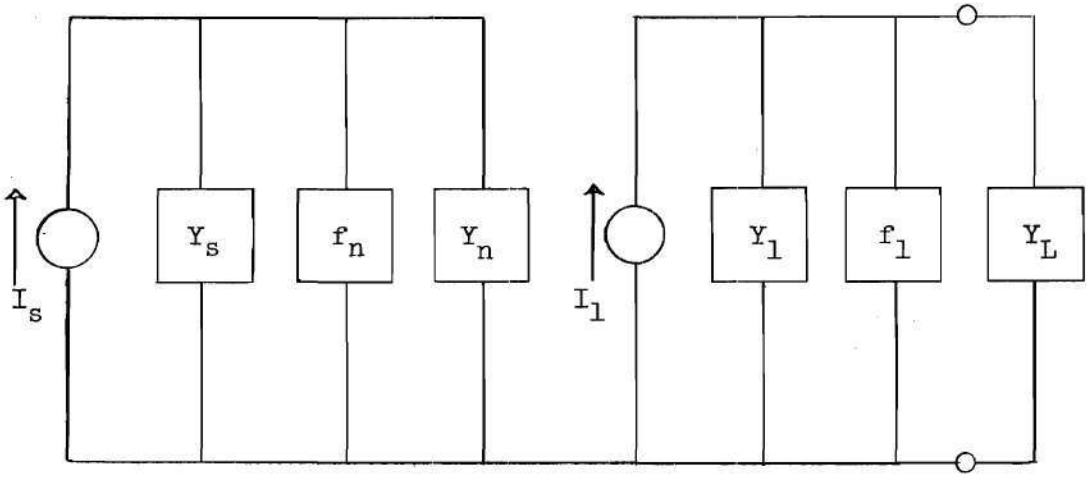


Figure 2C. Equivalent Circuit of the Series Limiter.

Now assuming that the normalized admittance seen by the load is

$y_1 = \frac{i_1}{v_1} = \frac{j\omega q_1}{v_1}$, and substituting

$q_1 = q_{1_r} + jq_{1_i}$, we obtain

$$y_1 = - \frac{\omega q_{1_i}}{v_1} + \frac{j\omega q_{1_r}}{v_1} \qquad (21C)$$

and combining (17C), (18C), and (21C)

$$y_1 = - \frac{n\omega\, \alpha_n v_1^{\,n-1}\, v_{n_i}}{v_1} + \frac{j\; n\omega\alpha_1 v_1}{v_1}$$

$$y_1 = - n\omega\, \alpha_n v_1^{\,n-2}\, v_{n_i} + j\; n\omega\,\alpha . \qquad (22C)$$

But we wish to determine y in terms of the input nω; therefore, we must express v_1 in terms of the input parameters.

If we assume that the tuned circuits are ideal then

$$q_{n_r} = \alpha_n v_1^{\,n} \tag{23C}$$

and

$$v_1 = (q_{n_r}/\alpha_n)^{1/n} . \tag{24C}$$

Also by the above assumption the reactive term in (22C) can be neglected (the circuits are resonated at the frequencies of interest).

Therefore, from (22C) and (24C),

$$v_{n_i} = \frac{y_1}{-n\omega\,\alpha_n\,(q_{n_r}/\alpha_n)^{1-(2/n)}} = \frac{g_1}{n\omega\,\alpha_n^{\,2/n}\quad q_{n_r}\,q_{n_r}^{-(2/n)}}$$

$$v_{n_i} = \frac{g_1}{n\omega\,\alpha_n^{\,2/n}} \quad q_{n_r}^{(2/n)-1} \tag{25C}$$

The normalized input conductance at the fundamental frequency is:

$$g_{in_n} = \frac{n\omega q_{n_r}}{v_{n_i}}$$

$$= \frac{n\omega q_{n_r}\,(n\omega\,\alpha_n^{\,2/n})}{q_{n_r}^{\,(2/n)-1}}$$

$$= \frac{n^2\omega^2\alpha_n^{\,2/n}\quad q_{n_r}^{\,(2-2/n)}}{g_1} \tag{26C}$$

Now we wish to unnormalize the expression for the limiter in which a semiconductor nonlinear capacitor is used. From experiment it has been determined that the capacitance is of the form

$$C\ (v) = C' + \frac{C_o'}{(1 - v/\Phi)^{\gamma}} \tag{27C}$$

where C' is an empirically determined value, C_o' is the capacity obtained as discussed in Appendix B, Φ is the contact potential and γ depends on the type of junction.

$$C\ (v) = \frac{dQ}{dv}$$

$$\therefore \quad Q = \int C' + \frac{C_o'}{(1 - V/\Phi)^{\gamma}} \quad dV$$

$$= C'V + \frac{C_o'}{1 - \gamma} \quad (1 - V/\Phi)^{1-\gamma}$$

$$= C'V + \frac{C_o'}{\Phi(1 - \gamma)} \quad (\Phi - V)^{1-\gamma}. \tag{28C}$$

If we separate the variables into static and ac components we obtain for Q_o:

$$Q_o = C'v_o + \frac{C_o'}{1 - \gamma} \quad V_o^{1-\gamma} \quad .$$

But $v + \quad = v_o + v_{ac}$, and $Q = Q_o + Q_{ac}$

$$\therefore \quad Q_o = C'\ v_o + \frac{C_o'}{1 - \gamma}\, v_o = (C' + C_o'/1-\gamma)\ V_o\ . \tag{29C}$$

We wish to unnormalized the expressions obtained for the equipment circuit. To do this we must use the following normalizing factors:

$v_n = \frac{V_n}{V_o}$, where V_n is the input voltage and V_o is the bias voltage.

$$q_n = \frac{Q_n}{Q_o} = \frac{Q_n\ (1 - \gamma)}{[C'(1-\gamma)+C_o']\ V_o} = \frac{I_n\ (1 - \gamma)}{\omega V_o\ [C'(1-\gamma)+C_o']}$$

$$g_n = \frac{(1 - \gamma)}{[C'(1-\gamma)+C_o']}\ G_n$$

$$g_1 = \overline{[C'(1-\gamma)+C_o']}\quad G_1$$

The input conductance becomes

$$G_{in_n}\frac{(1-\gamma)}{[C'(1-\gamma)+C_o']} = \frac{n^2\omega^2\ \alpha_n^{\ 2\ n}}{\frac{(1-\gamma)\ G_1}{[C'(1-\gamma)+C_o']}}\left\{\frac{I_n(1-\gamma)}{\omega v_o[C'(1-\gamma)+C_o']}\right\}^{2-2\ n}$$

$$G_{in_n} = \frac{n^2\ \alpha_n^{\ 2/n}\ \omega^2\ [C'\ (1-\gamma)\ +\ C_o']^2}{(1\ -\ \gamma)^2\quad G_1}\left\{\frac{I_n(1\ -\ \gamma)}{2\omega v_o[C'(1-\gamma)+C_o']}\right\}^{2-2/n} \tag{30C}$$

where the equivalent circuit can be drawn as shown below.

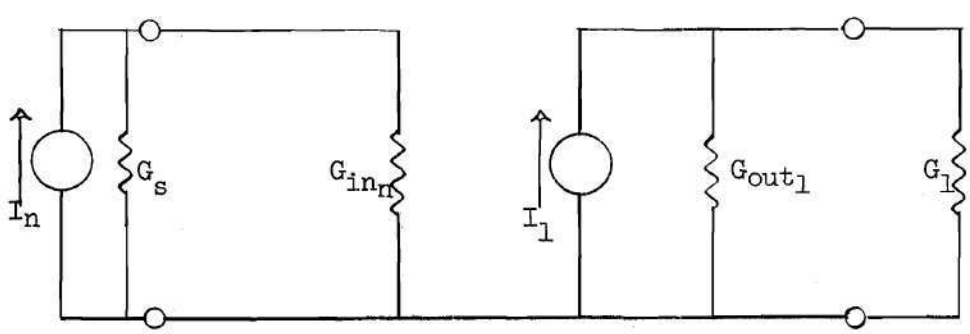


Figure 3C. Equivalent Circuit of Series Limiter.

For the case of n = 2, the input conductance will reduce to:

$$G_{in} = \frac{4\omega^2 \alpha_2^2 \; [C'(1-\gamma)+C_o']^2}{(1-\gamma)^2 \; G_1} \left\{ \frac{I_2 \; (1-\gamma)}{\omega V_o \; [C'(1-\gamma)+C_o']} \right\}$$

Since $$\alpha_2 = \frac{C_o'}{[C'(1-\gamma) + C_o'] \; (1-\gamma)}$$

$$G_{in} = \frac{2\omega(C_o')^2(1-\gamma)^2 \quad I_2}{G_1 v_o \; [C'(1-\gamma) + C_o']} \tag{31C}$$

$$E_{in} = \frac{I_2}{G_{in}} = \frac{[C'(1-\gamma) + C_o'] \; G_1 v_o}{2\omega(C_o')^2(1-\gamma)^2} \tag{32C}$$

It will be noted that the input voltage for the circuit is constant if a voltage exists at ω, i.e., if ω exists. This equation also indicates that the threshold of limiting decreases with decreased bias, and increased C_o. This effect would be expected from observation of the curve of capacitance versus bias since the largest change in capacitance for the smallest charge in voltage occurs in the low bias region. It must be remembered, however, that the mode of operation charges when the applied signal exceeds the bias voltage.

Analysis of the Shunt Limiter Circuit.-- Solutions leading to the circuit equations for the series limiter circuit involve the solution for the various voltages (Equation 10C) in terms of the driving voltage.

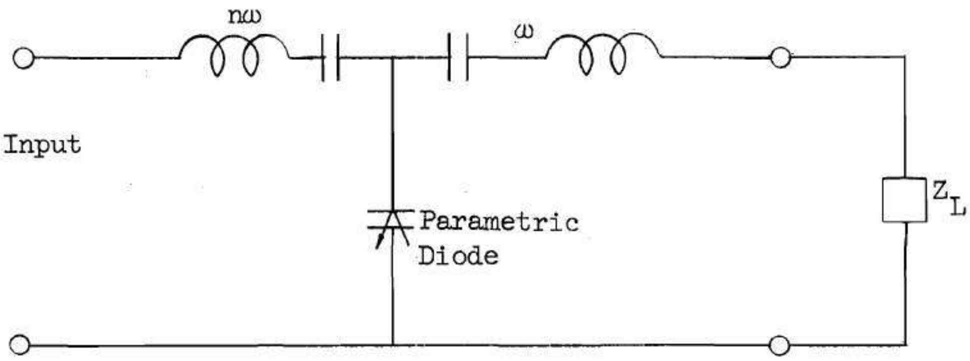


Figure 4C. Shunt Limiter Circuit.

Since, as in the case of the series limiter, we need to consider only the first and n-th terms of the Fourier Series for the voltage, it reduces to:

$$v = \beta_1 q + \beta_n q^n , \tag{33C}$$

Now q^n can be replaced by its complex Fourier series represented by

$$q^n = \sum_{n=-\infty}^{\infty} (q^n)_n \, \epsilon^{jn\omega t}, \tag{34C}$$

where $(q^n)_n$ is evaluated as in equation (12C). The resulting frequency components of interest are:

$$v_1 = \beta_1 q_1 + \beta_b (q^n), \tag{35C}$$

$$v_n = \beta_1 q_n + \beta_n (q^n)_n \quad . \tag{36C}$$

As in the voltage case we allow $q_1 = q_{-1}$ (where q is real); and separate (36C) and (37C) into the real and imaginary parts, which results in:

$$v_{1_r} = \beta_1 q_1 \tag{37C}$$

$$v_{1_i} = n\beta_n q_1^{\,n-1} q_{n_i} \tag{38C}$$

$$v_{n_r} = \beta_1 q_{n_r} + \beta_n q_1^{\,n} \tag{39C}$$

$$v_{n_i} = \beta_1 q_{n_i} \tag{40C}$$

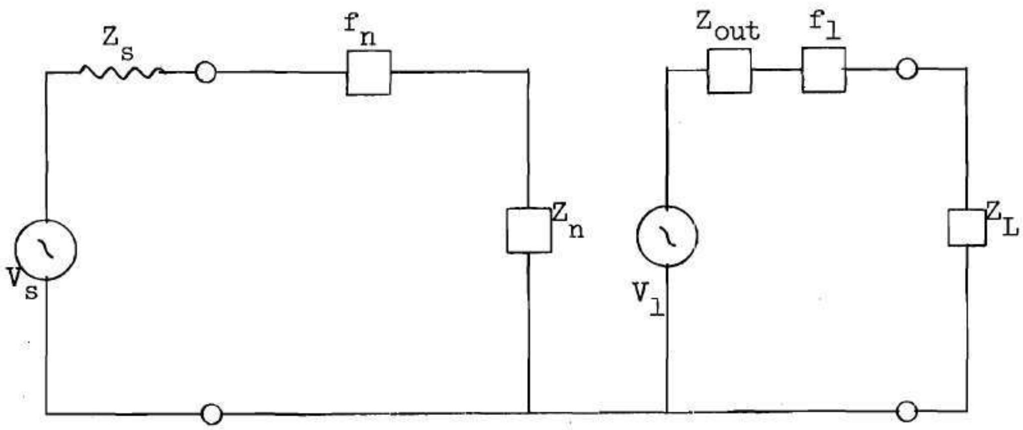


Figure 5C. Equivalent Circuit of the Shunt Limiter.

If we assume that the input and output circuits are resonant as before in the case of the series limiter, we can write:

$$v_{n_r} = \beta_n q_1^{\,n} \tag{41C}$$

and

$$q_1 = (v_{n_r} / \beta_n)^{1/n} .$$

Now if we assume that $z_1 = v_1/i_1$ where $z_1 = z_{out} + z_L$

$$z_1 = -\frac{jv_1}{\omega q_1} = \frac{v_{1_i}}{\omega q_1} - j\,\frac{v_{1_r}}{\omega q_1} \tag{42C}$$

But by the previous assumption that the circuits are resonant we can neglect the reactive term, which leaves

$$z_1 = \frac{v_{1_i}}{\omega q_1}$$

or

$$z_1 = \frac{n\beta_n {q_1}^{n-1} q_{n_i}}{\omega q_1}$$

$$q_{n_i} = \frac{\omega q_1 z_1}{n\beta_n {q_1}^{n-1}} \tag{43C}$$

The normalized input impedance at the fundamental frequency is

$$z_{in} = \frac{v_{n_r}}{n\omega q_{n_i}}$$

$$z_{in} = \frac{n v_{n_r} \beta_n {q_1}^{n-1}}{n\omega^2 q_1 z_1}$$

$$= \frac{v_{n_r} \beta_n {q_1}^{n-2}}{\omega^2 z_1}$$

Now substituting for q_1 in terms of the input we can obtain:

$$z_{in} = \frac{v_{n_r}\beta_n}{\omega^2 z_1} \quad (v_{n_r} / \beta_n)^{1-2/n}$$

$$= \frac{\beta_n^{\ 2/n}}{\omega^2 z_1} \quad v_{n_r}^{\ 2-2/n} \tag{44C}$$

We wish now to unnormalize (44C) in terms of the nonlinear capacitor. We therefore use the normalizing factors:

$$v_n = \frac{V_n}{V_o}, \quad z_1 = \frac{[C'(1-\gamma) + C_o']}{(1 - \gamma)} \ Z_1$$

and

$$z_{in} = \frac{[C' \ (1-\gamma) + C_o']}{(1 - \gamma)} \quad Z_{in}$$

which were derived in the previous section.

Therefore,

$$Z_{in} = \frac{\beta_n^{\ 2/n} \ (1-\gamma)^2}{\omega^2 z_1 \ [C'(1-\gamma)+C_o']^2} \quad (V_n/V_o)^{2-2/n} \tag{45C}$$

and for n = 2, (45C) becomes

$$Z_{in} = \frac{\beta_2 \ (1-\gamma)^2 \ \ V_2}{\omega^{\ 2} V_o Z_1 [C'(1-\gamma)+C_o']^2} \quad .$$

Now solving for β_2 we obtain

$$\beta_2 = \frac{[C'(1-\gamma)+C_o'] \quad (1-\gamma)}{C_o'}$$

which when combined with (45C) for the case of n = 2 gives

$$Z_{in} = \frac{(1 - \gamma)^3}{\omega^2 V_o Z_1 C_o' \, [C'(1-\gamma) + C_o']} \tag{46C}$$

Now using (46C) to obtain the input current, we obtain

$$I_{in} = \frac{\omega^2 V_o R_1 C_o' \, [C' (1-\gamma) + C_o']}{(1 - \gamma)^3} \tag{47C}$$

It will be noted that the input current is constant if the circuit oscillates and a current actually exists at the half frequency. Furthermore the limiting value is directly proportional to the frequency and bias voltage.

APPENDIX D

GLOSSARY OF SYMBOLS AND ABBREVIATIONS

α_k - Coefficients of the Taylor Series representation for Q.

α_i - Coefficients from the statistical analysis for C(v).

α - Constant gradient for the impruity density.

A - Coefficients of the v_n term.

$\overline{A}_1$ - Electrical oscillation amplitude.

$\underline{A}$ - Cross-section area (plate area).

B - Coefficient of the v_1^n term.

$\overline{B}$ - Mechanical resistance.

β_k - Coefficients of the Taylor Series representation of V.

C - Capacitance.

C_a - Fixed dc isolation capacitor (.01 μfd silver mica).

C_b - Fixed capacitor for determining L of the tuned circuit.

k_i - Normalizing constants used in fitting the empirical curve.

C_p - Equivalent parallel capacitance.

C_s - Equivalent series capacitance.

C_{sc} - Space charge capacity.

C' - Empirical correction factor(capacitance).

C_1 - Capacity at $V + \Phi = 1$.

C_o - C(v) evaluated for v = 0.

C_o' - Empirically determined C_o.

C(v) - Capacitance as a function of voltage.

$C(t)$ - Capacitance as a function of time.

d - Plate separation.

db - Decibel.

dc - Direct current.

e - Electronic charge.

ϵ - Dielectric constant.

E_{in} - Input voltage.

f - Frequency.

f_c - Cutoff frequency.

f_1 - Input frequency.

f_2 - Idler frequency.

f_3 - Idler frequency.

f_o - Output frequency.

f_p - Pump frequency.

f_s - Signal frequency.

f_{ls} - Lower sideband frequency.

f_{us} - Upper sideband frequency.

F_i - Statistic associated with each term of the power series.

F^* - Critical statistical value from tables.

F_m - Mechanical driving force.

g_1 - Normalized conductance seen by the load.

g_n - Normalized conductance at frequency $n\omega$.

g_{in_n} - Normalized input conductance.

G_a - Equivalent output loss conductance due to the output filter and parametric diode.

G_b - Equivalent input loss conductance due to the input filter and parametric diode.

G_p - Power gain.

G_l - Total equivalent load conductance.

G_{in} - Equivalent input conductance.

γ - Constant determined by the junction characteristics.

i - Imaginary.

i_n - Current at frequency $n\omega$.

i_1 - Current at frequency ω.

I_n - Unnormalized current at frequency $n\omega$.

I_{in} - Input current.

I_2 - Current for special case of $n = 2$.

K - A constant.

k - Integer 1, 2, 3, ...

L - Inductance

L_a - n_i/a.

L_o - Debye length.

λ - Phase angle.

m - Integers 1, 2, 3, ...

mc - Megacycle.

mv - Millivolt.

mw - Milliwatt.

MS - Mean square.

n - Integers 1, 2, 3, ...

n_i - Electron density.

pf - 10^{-12} farads.

$p_j(x)$ - Normalized polynomials.

P_{in} - Input power.

$P\,\omega$ - Power at the frequency ω.

q - Normalized variation of charge.

q_1 - Charge at frequency ω.

q_n - Charge at frequency $n\omega$.

Q - Total charge.

$\underline{Q}$ - Figure of merit.

Q_o - Quescent value of charge.

Q_n - Total charge at frequency $n\omega$.

Φ - Contact potential.

r - Real.

rf - Radio frequency.

R - Circuit resistance.

R_l - Load resistance.

R_p - Parallel equivalent resistance of the capacitor.

R_s - Series equivalent resistance of the capacitor.

RX - Resistance - reactance.

SS - Sum square.

θ - Phase angle.

t - Time.

v - Normalized variation of V.

$v(t)$ - Voltage as a function of time.

v_1 - Voltage at frequency ω.

v_2 - Voltage for case of $n = 2$.

v_n - Voltage at frequency $n\omega$.

V - Total voltage.

V_o - Quescent value of voltage across the junction.

VTVM - Vacuum tube voltmeter.

ω - Radian frequency.

W_o - Power at the output frequency.

W_1 - Power at the input frequency.

$W_{m,n}$ - Average power at a frequency determined by $f = \pm \left|mf_1 + nf_o\right|$.

X_c - Capacitive reactance.

x - V

x' - Coded value of V.

y_1 - Normalized admittance seen by the load.

y - Empirically determined C(v).

y_n - Normalized input admittance.

Z_1 - Output impedance.

Z_{in} - Input impedance.

z_n - Normalized input impedance.

z_1 - Normalized impedance seen by the load.

ξ_i - Unnormalized orthogonal polynomials.

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